

**CS 150 Fall 1991  
Midterm 2  
Professor Randy H. Katz**

**Problem #1 (5 Credits)**

Circle T for true and F for false about each of the following statements (1 point each):

T F A Moore finite state diagram is converted to a Mealy state diagram as follows. Each Moore state is replaced by a Mealy state. Then all transitions in the Mealy state diagram are the same as those in the Moore state diagram. Finally, the Moore state output is associated with all input transitions to its equivalent Mealy state.

T F The 74163 is internally implemented as a ripple counter with a load and clear capability.

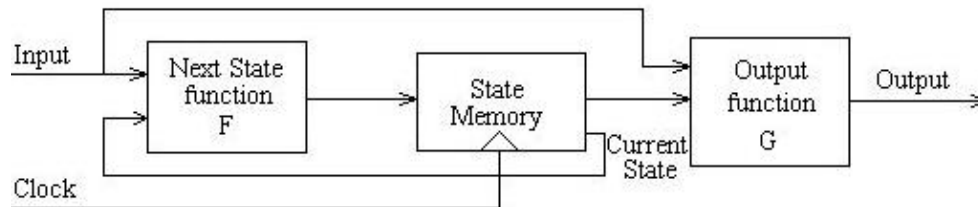
T F When a latch is enabled, outputs will always change in response to input change assuming that set-up and hold time constraints are met.

T F A ring counter (also known as a Johnson counter) with n-flip-flops cycles through unique states during normal operation.

T F A state machine with n inputs, m outputs, and p flip-flops has  $2^{(n+m)}$  states.

**Problem #2 (10 Credits)**

A clocked synchronous state machine is built as shown below.



The next state logic F is a combinational circuit with a maximum propagation delay of  $t_F$ . The state memory is an edge-triggered register with a minimum clock-to-output propagation delay of 0 and a maximum propagation delay of  $t_R$ , a setup time of  $t_S$ , and a hold time of  $t_H$ . The output logic G is a combinational circuit with maximum propagation delay of  $t_G$ .

What is the maximum clock frequency at which the machine will cycle through its states properly?

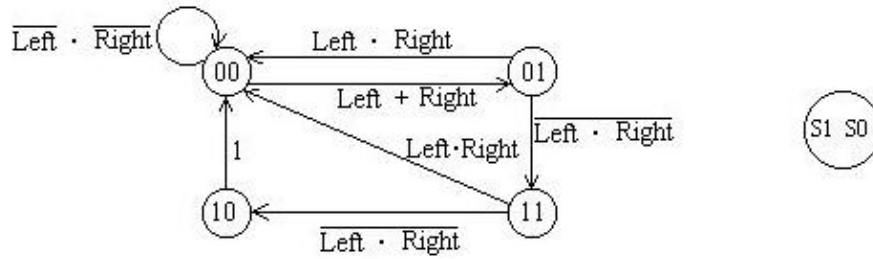
What is the minimum propagation delay required for the proper operation of the next state logic F?

What is the maximum delay from triggering clock edge until the output is valid?

Is this a Mealy or a Moore finite state machine?

**Problem #3 (10 Credits)**

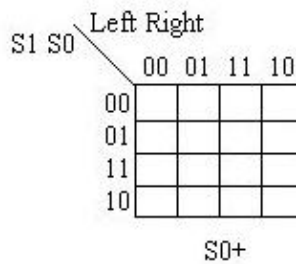
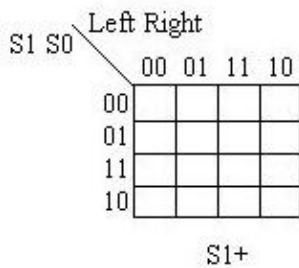
Given the following state diagram:



Complete the State Transition Table (4 points):

Current State		Input		Next State	
S1	S0	Left	Right	S1+	S0+

Fill in the K-Maps(4 points):

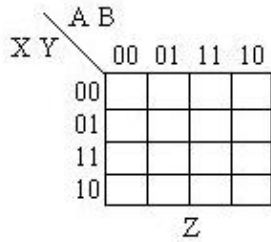
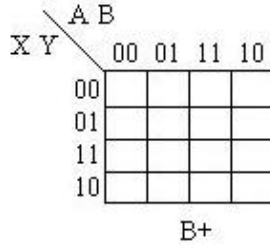
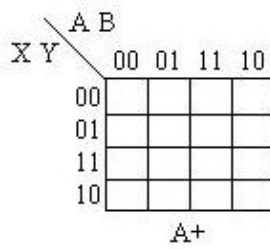


Minimized Next State Equations (2 points):

S1+ =

S0+ =



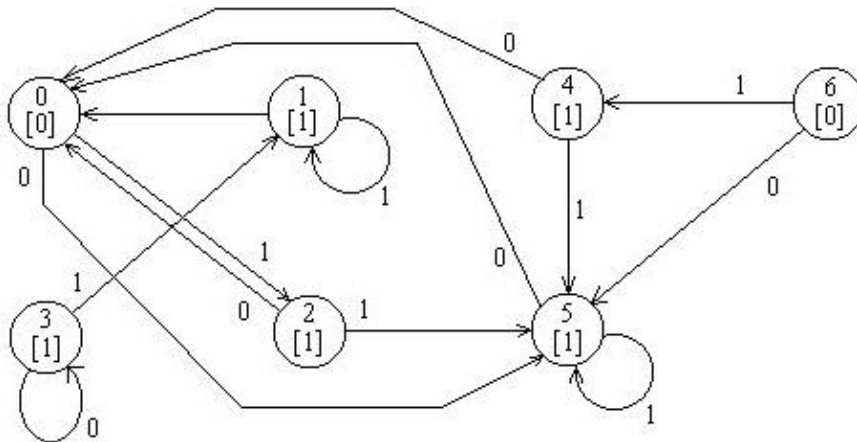


Complete the State Transition Table (4points):

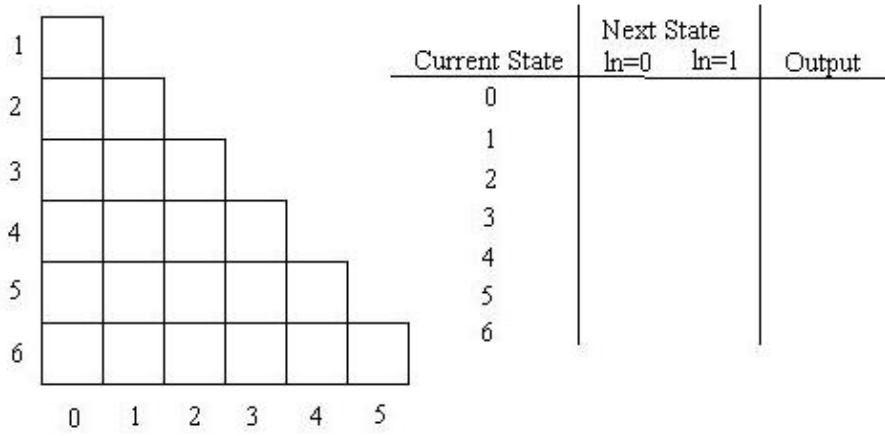
Current State		Next State				Output Z			
		XY=00	XY=01	XY=10	XY=11	XY=00	XY=01	XY=10	XY=11
A	B	A+ B+	A+ B+	A+ B+	A+ B+				
0	0								
0	1								
1	0								
1	1								

**Problem #5 (20 Credits)**

Starting with the following state diagram and state transition diagram:



Fill in the State Transition Table and Implication Chart below (5 points):



Using the implication chart, which of the original states can be combined? (15 points)

### Problem #6 (30 Credits)

You are to design the state diagram for a simple controller that turns a lamp on and off at preset times. We call this a timed light switch. The finite state machine has six input RESET, SetTime, SetLiteOn, SetLiteOff, RUN, and ADVANCE. The first five inputs are generated by a five position rotary switch that advances through RESET, SetTime, SetLiteOn, SetLiteOff, and RUN (the inputs are mutually exclusive and are encountered in the specified order). The ADVANCE input is a push button. See the figure below. When the user holds the ADVANCE button down (asserted), the displayed time rapidly advance through twenty four hours, a minute at a time.

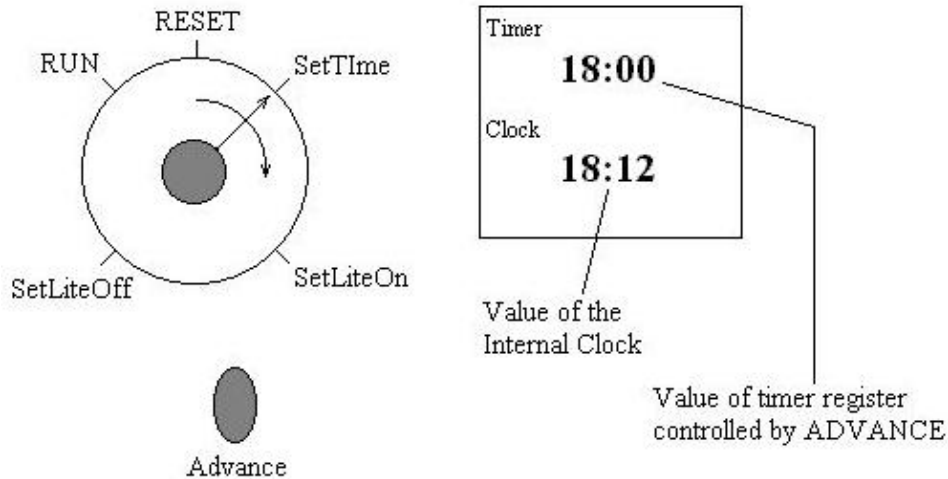
The typical operation of the timed light switch works as follows. It is normally in RUN mode. The lamp is turned on whenever the internal clock matches an internal register (LiteOn) that holds the time to turn the light on. The lamp is turned off whenever the internal clock matches an internal register (LiteOff) that holds the time to turn the light on.

To operate the timed light switch, you must first set the current time, next the time on, and finally the time off. This is accomplished as follows. The mode switch is moved from RUN to RESET. This causes an internal timer register to be loaded with the time 08:00. Next, the mode switch is moved to the SetTime position. Whenever ADVANCE is pushed and held down, the timer register rapidly cycles through the minutes and hours. The consumer wants "pulse" or single step ADVANCE as it gets close to the current time. By moving the switch to SetLiteOn, the current value in the timer register overwrites the value in the internal clock register. At the same time, the internal timer register is reset to 08:00.

By working with the ADVANCE button, the consumer sets a new time at which the light is to be turned on. Moving the mode switch to SetLiteOff causes the LiteOn register to be overwritten by the time register.

Using the ADVANCE button once again, the consumer advances the timer from its latest value (the "lights on" time) to the desired time to turn the lights off.

Once the mode switch is set to RUN, the timed light switch goes into its running mode.



---

**Posted by HKN (Electrical Engineering and Computer Science Honor Society)  
Univeristy of California at Berkeley  
If you have any questions about these online exams  
please contact [examfile@hkn.eecs.berkeley.edu](mailto:examfile@hkn.eecs.berkeley.edu).**