Name_____

SID_____

EECS150
Midterm1
2/16/06

| 1&2 | | /20 |
|---|---|---|
| 3 | | /20 |
| 4 | | /15 |
| 5 | | /20 |
| 6 | | /25 |
| Total | | /100 |

1) Given **F=AB+CD'**
   a. Implement F using as few 2 input NAND gates as possible. Assume that only the true literals (A,B,C,D) are available, not their complements (A', B', C', D').

   b. Write **F'** in product of sums notation

2) Given **G = (A+B)(C'+D)**
   a. Implement G using as few 2 input NOR gates as possible. Assume that only the true literals are available, not their complements.

   b. Write **G'** in sum of products notation.

3) Answer the following questions for the FSM below:
   a. Is this a Mealy or a Moore machine?
   b. Briefly describe the function of this sequence detector. When is the output 1?


   c. Write a Verilog module which would implement this FSM for input variable "In" and output variable "Out." Use the same standard format as was presented in the Lab 3 lecture and used in Lab 3. (Define your states; use one always block for next state and output; use one always block for state transition)

Reset ─── Sue / 0 ⟲ 0

0

Bob / 0 ⟲ 1

Ken / 1

1

1

0
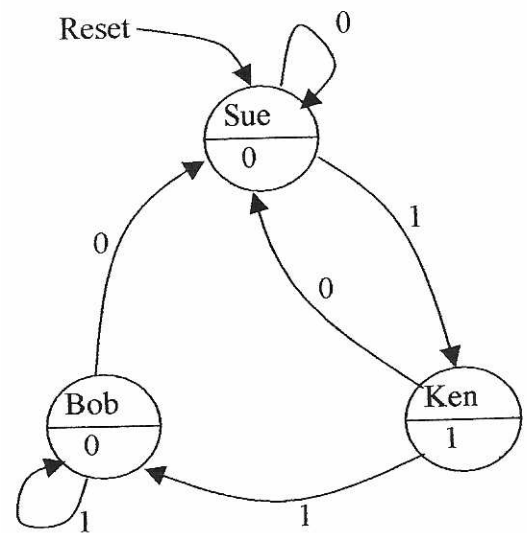
4) For the following questions, assume that only the true variables (A,B,C) are available, and not their complements. Try to use the fewest gates and the fewest inputs possible.

a. Implement the function $F(A,B,C) = \Sigma m(0,1,4,7)$ using a 4:1 mux and at most 1 inverter.

b. Use a 3:8 decoder and OR and AND gates to implement $F(A,B,C) = \Sigma m(0,4,7)$

c. Use a 3:8 decoder and OR and AND gates to implement $G(A,B,C) = \Pi M(1,6)$

5) Design a counter with one control input. When the input is high, the counter
   should sequence through three states: 10, 01, 11 and repeat. When the input is low
   the counter should sequence through the same states in the opposite order 11, 01,
   10 and repeat.
   a. Draw the state diagram and state transition table
   b. Implement the counter using D flip flops and whatever gates you like.
   c. Is your counter self-starting with the input either high or low?

6) [25pts]
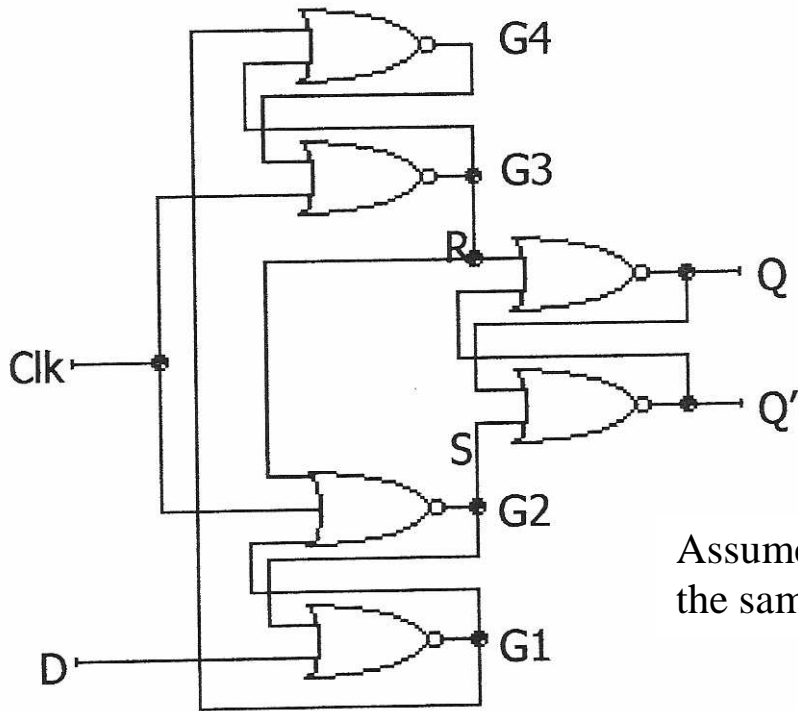


Assume all gates have exactly the same delay.

1 gate delay

Clk

D

G1

G2

G3

G4

Q

Q'