Your Name: _____ **SID Number:** _____

UNIVERSITY OF CALIFORNIA AT BERKELEY

BERKELEY • DAVIS • IRVINE • LOS ANGELES • RIVERSIDE • SAN DIEGO • SAN FRANCISCO SANTA BARBARA • SANTA CRUZ

Department of Electrical Engineering
and Computer Sciences

CS 150 - Spring 1997
Prof. A. R. Newton

(1)	/40
(2)	/40
(3)	/60
TOTAL	**/140**

Quiz 2

Room 10 Evans Hall, 2:10pm Tuesday April 8th
(Open Katz only, Calculators OK, 1hr 20mins)

Include all final answers in locations indicated on these pages and in pen. Use space provided for all working. If necessary, additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

1. (a) Convert the **BCD coded number** below to equivalent decimal form:

   1000011101100010.01100101

   (b) Convert $(271.A)_{16}$ to (i) **Base 2** and (ii) **Base 8** equivalents.

   (c) Design a circuit for **converting a 4-bit Gray code into its binary equivalent**. You may use **AND, OR, XOR, c inverter gates only**. Use as few gates as possible.

   (d) Implement a **1-bit full adder** using a **minimum number of 4-input, two control-line multiplexers and inverter only**. An inverter counts as 1/5th (20%) of a MUX. **Assume complements are not available.**

1 (a) (10pts)

$1000011101100010.01100101_{BCD}$ = _____$_{10}$

(b) (10pts)

$(271.A)_{16}$ = _____$_2$

_____$_8$

(c) (10pts) Schematic diagram of code converter:

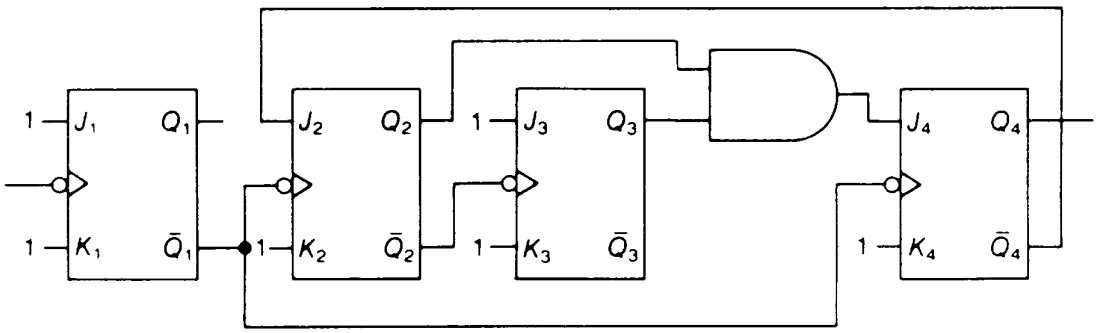
(d) (10pts) Schematic diagram of 1-bit full adder:

Additional space for Problem 1

Your Name: _____

(2) (40 points)

(a) Describe the function and characteristics of the counter circuit shown below:



2(a) (20pts)

What is its function? .....

.....

.....

.....

.....

.....

.....

.....

.....

.....

A **JN flip-flop** has **two inputs, J and N**. Input J behaves like the J input of a JK flip-flop, and **N behaves like the complement of the K input** of a JK flip flop (i.e. $N = \overline{K}$).

(i) Obtain the **characteristic table** of the JN flip-flop

(ii) Show that by connecting the two J and N inputs together, one obtains a D-type flip-flop.

(i) (10pts) Characteristic Table:

(ii) (10pts) Proof of characteristics with two inputs connected:

Additional space for Problem 2

Your Name: _____

(3) As usual, for the following problems, ***be sure to state all assumptions clearly***.

(a) Obtain the **reduced flow table** for the primitive flow table shown opposite.

(b) Obtain the **primitive flow table for a negative edge-triggered T flip-flop**. Consider T as a regular input, C as its clock input, and Q as its output. **Do not merge the table.**

x_1x_2			
00	01	11	10
(1)	5	6	2
1	—	—	(2)
—	5	(3)	2
(4)	5	3	—
—	5	(6)	2
4	(5)	—	—

3(a) (10pts)Reduced Flow table:

(b) (20pts) Primitive flow table for edge-triggered T flip-flop:

Continued on following page

(3) (c) Design a **circuit that outputs a short pulse on output Z each time an input variable, X, makes a 0® 1 or a 1® 0 transition**. Use **as few states as possible**. Show **the next-state and output equations for your circuit** in as compact form as possible.

(d) Obtain a **race-free state-assignment** for the merged flow table shown opposite, **using as few additional states as possible**. **Be sure to include a transition graph**. **List all state codes**. Assume the outputs are such that no further merging is possible. Assume the outputs can be chosen to avoid glitches.

	x_1x_2		
00	01	11	10
(1)	(2)	3	4
7	(6)	(3)	5
(7)	6	(8)	(4)
7	2	3	(5)

3(c) (20pts) Next-state and output equations:

_____

_____

_____

Z =_____

3(d) (10pts)

Transition graph:

State Codes:

_____

_____