Your Name: _____Discussion Section_____

CS150 Spring 1998

Quiz 1

Room 10 Evans Hall, 2:10pm Tuesday February 24

(Open Katz only, Calculators OK, 1hr 20mins)

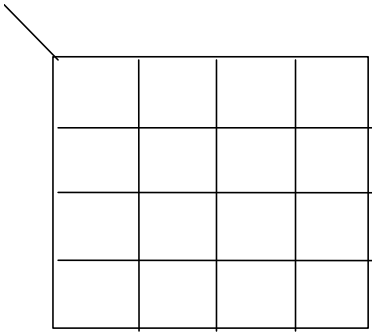
Include all final answers in locations indicated on these pages. Use space provided for all working. If necessary, attach additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

(1) (20pts) Consider the following logic function

$f(A,B,C,D) = \Sigma m(5,7,9,13) + \Sigma d(0,1,2,8,14,15)$

(a) Construct a **Karnaugh Map** and write the **Boolean expression for the function as a minimum sum-of-products realization** (minimum number of (gates + gate inputs.)) **Indicate the specific implicants** you have chosen to implement each function by **circling them on the maps.**

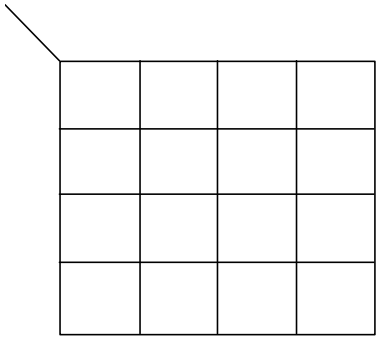
1(a) 5pts



f(A,B,C,D) = _____

(b) Construct a **Karnaugh Map** and write the Boolean expression for the function as a minimum **product-of-sums realization** (minimum number of (gates + gate inputs.)) **Indicate the specific implicants** you have chosen to implement each function by **circling them on the maps.**

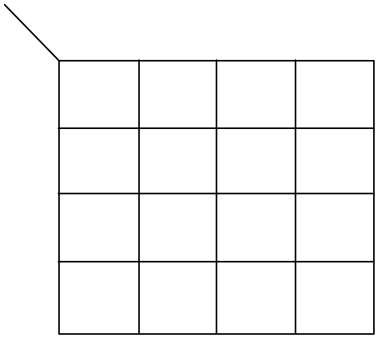
1(b) 5pts



f(A,B,C,D) = _____

(c) **Consider a function f(A,B,C,D) = Σm(0,2,4,5,8,10,11,15)**, construct a **Karnaugh map** and write the **Boolean expression for the function as a minimum sum-of-products realization**

1(c)5pts

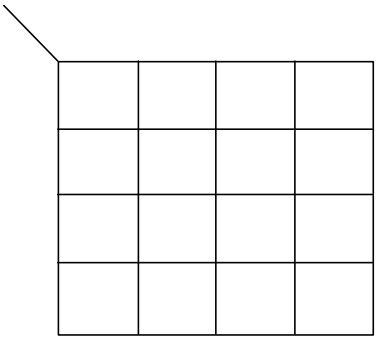


f_1(A,B,C,D) = _____

d) How many static-1 hazards are there in your minimum sum-of-products realization? How would you change your circuit to remove them?

1(d)5pts # hazards=_____

My fix is (describe and illustrate on K-map):



Additional space for Problem 1

Your Name: _____Discussion Section_____

(2) (25pts) Implement the function **f(A,B,C,D) = AB+C'D'** using ***only:***
(a) 2 input AND and OR gates and inverters**.**

2(a) (5pts)

(b) 2 input NAND gates

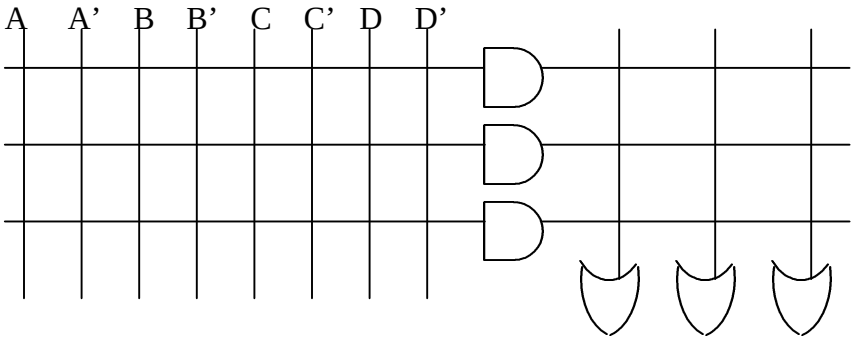
2(b) (5pts)

(c) 2 input NOR gates

2(c) (5pts)

(d) an AND/OR PLA

2(d) (5pts)



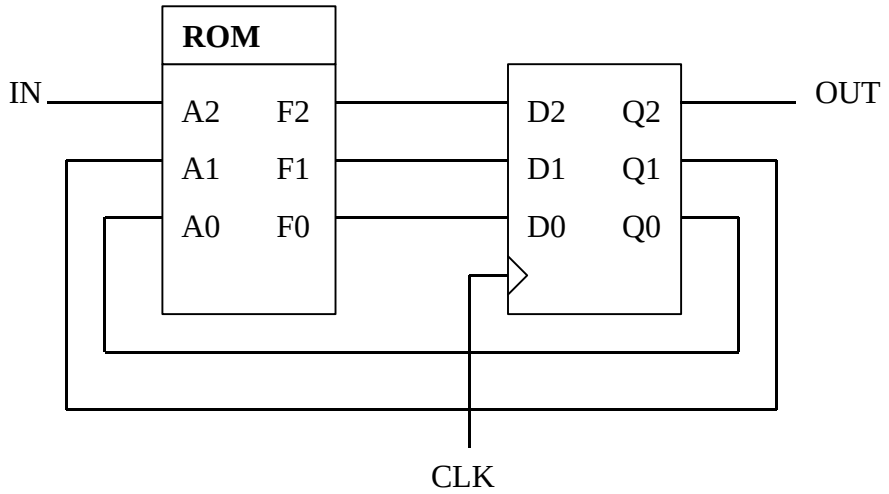
(e) If the function were implemented using a ROM, **how many ROM storage locations** would be required? **How many address input lines** would the ROM have?

2(e) (5pts)

Storage Locations: _____ **Address inputs: _____**

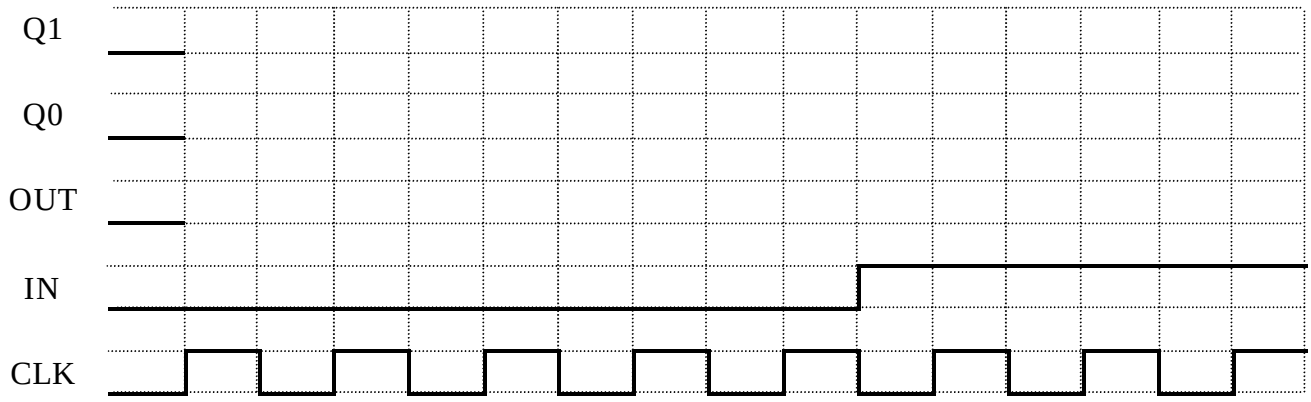
Additional space for Problem 2

(3) (20pts) Given the ROM-based FSM below,



A2	A1	A0	F2	F1	F0
0	0	0	1	0	1
0	0	1	0	1	1
0	1	0	1	1	1
0	1	1	1	1	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	1	0	0

(a) draw the waveforms for Q1, Q0, and OUT. You may assume that the clock period is long compared to the gate delays in the components.



(4) (25pts) Design a Mealy FSM with one input and one output. When the input is high, the FSM should cycle through the states 0,1,2,0,1,2 … (count up) and when the input is low the FSM should cycle through the states 0,2,1,0,2,1 … (count down) The output should be one when the machine makes a transition into state 0. State 3 should always transition to state 0.

a) Draw the state transition diagram and generate a state transition table:

b) Determine the next-state and output equations and implement the design using positive edge triggered D flip-flops.

4(a) (10pts)

4(b) (15pts)