Microelectronic Devices and Circuits- EECS105
Final Exam

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Your Name: OFFICIAL SOLUTIONS
(last) *(first)*

Your Signature: _____

1. Print and sign your name on this page before you start.
2. You are allowed three, 8.5"x11" handwritten sheets. No books or notes!
3. Do everything on this exam, and make your methods as clear as possible.
4. Always show the expression before you do the final calculation. A correct expression is worth 70% of the credit. A correct calculation gets tou you the remaining 30%.

Problem 1	_____	*/ 40*
Problem 2	_____	*/ 25*
Problem 3	_____	*/ 35*
TOTAL	_____	*/ 100*

MOS Device Data[1] (you may not have to use all of these...)
$\mu_n C_{ox} = 50\mu A/V^2$, $\mu_p C_{ox} = 25\mu A/V^2$, $V_{Tn} = -V_{Tp} = 1V$, Lmin = $2\mu m$. $V_{BS} = 0$.
$\lambda_n = \lambda_p = 0.1V^{-1}$ when L = $1\mu m$, and it is otherwise proportional to 1/L
$C_{ox} = 2.3fF/\mu m^2$, $C_{jn} = 0.1fF/\mu m^2$, $C_{jp} = 0.3fF/\mu m^2$, $C_{jswn} = 0.5fF/\mu m$,
$C_{jswp} = 0.35fF/\mu m$, $C_{ovn} = 0.5fF/\mu m$, $C_{ovp} = 0.5fF/\mu m$
BJT Device Data (you may not have to use all of these...)
$\beta_f = 100$, $I_S = 10^{-17}A$, $V_{CE\,SAT} = 0.1V$, $V_A = 25V$, $\tau_F = 50ps$, $C_{je} = 15fF@V_{BE} = 0.7V$,
$C\mu = 10fF@V_{BC} = -2.0V$

[1] Except as indicated on the particular problem...

Problem 1 of 3: Answer each question briefly and clearly. (40 points)

1.1 Why circuit nodes with very high impedance matter in terms of frequency response? (4pts)

because they contribute a large RC term...

1.2 When we say that an amplifier stage is "broadband", what do we mean? (4pts)

It is only limited by the f_T of the device (no Miller effect)

1.3 Place check marks where appropriate (4pts)

Amp Type	Check if Broadband	Check if high R_{in}	Check if high R_{out}
CS		✓	✓
CD	✓	✓	
CG	✓		✓
CE			✓
CC	✓	✓	
CB	✓		✓

1.4 Choose the most appropriate answer (3pts)
The Open-Circuit Time Constant method can only work properly if:

- (o) … there is one dominant pole and no zeros (actually, zeros are OK if they happen at frequencies much higher than ω_0...)
- ( ) … there is an Open Circuit connection
- ( ) … there is no Miller Capacitance
- ( ) … the Time is Constant.

1.5 In this class we talked about the Miller Approximation. Why is it "approximate"? (4pts)

because we ignored the current drawn by the Miller cap by the output node.

1.6 Match the SPICE control cards (for the types of analysis) to the plots. (3pts)

(a) .DC → Figure 1
(b) .AC → Figure 2
(c) .TRAN → Figure 3

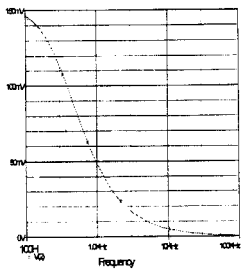


Figure 1

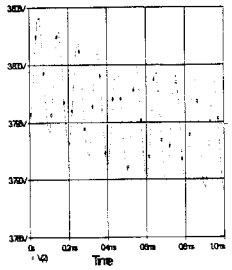


Figure 2

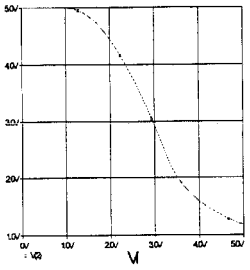
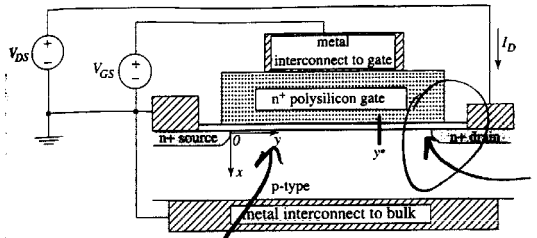


Figure 3

1.7 For the n-channel MOS transistor shown below, please mark the two ends of the channel (near the source and near the drain) and indicate whether or not each must be inverted so that this device is in saturation. (4pts)



1.8 What is the "law of the junction" and when does it apply? (4pts)

Law of the junction formula:
$p_n(x_n) = p_{no}\, e^{V_D/V_{th}}$
$n_p(-x_p) = n_{po}\, e^{V_D/V_{th}}$

The basic assumption behind it is…

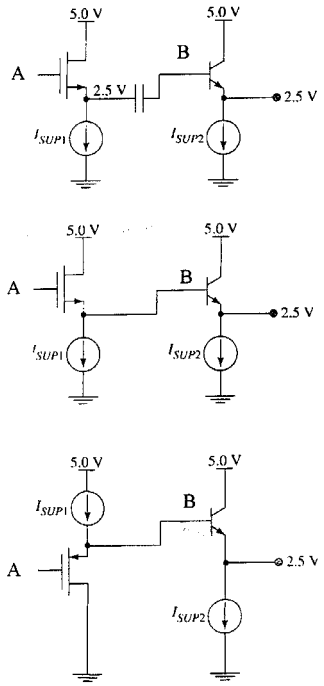
low-level injection.

1.9 What are the two (small signal) capacitive components of a forward biased junction? (4pts)

Symbol of first capacitance: depletion capacitance C_j
Verbal Definition:

Symbol of second capacitance: C_{diff}.
Verbal Definition: diffusion capacitance

1.10 For each of these circuits, calculate the "no-signal" DC-bias point at the nodes A and B, assuming that every MOS device is biased so that V_{GS}=1.5V and every BJT is biased so that V_{BE}=0.7V. After you have done that, circle the circuit that is the "best" in terms of voltage swing at the input A[2] *and* low frequency response, and explain where the other two fall short. (6pts)

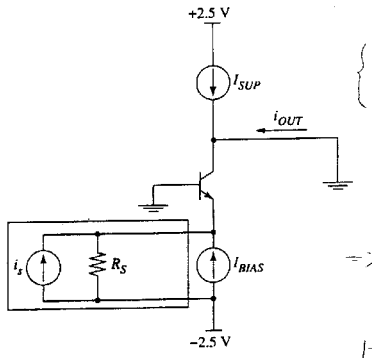


	Best	Explain Performance Limitation
V_A = 4 V_B = 3.2		$V_{out,max}$ = 3.5 V $V_{out,min}$ = 0.3 V V_A = 4 (not centered) Coupling Cap a problem
V_A = 4.7 V_B = 3.2		$V_{out,max}$ = 2.8 V $V_{out,min}$ = 0.5 V V_A = 4.7 (not centered)
V_A = 1.7 V_B = 3.2	✓	$V_{out,max}$ = 3.8 V $V_{out,min}$ = 0.8 ✓ V_A = 1.7 (good!) (almost centered)

[2] Note that the input voltage should not be allowed to go over 5V during the operation of these amps. Assume that all the current sources in this question have a minimum voltage drop of 0.5V.

Problem 2 of 3: Answer each question briefly and clearly. (25 points)

2.1 Design a Common Base "current buffer" amplifier stage so that it meets the following constraints: Total R_{out} > 20MΩ if R_s = 50kΩ, and an absolute current gain i_{out}/i_s greater than 0.99, when the stage output is shorted. (Use the simplified formulae that assume that $g_m r_o >> 1$, r_π, $r_o >> 1/g_m$, $r_o, r_{oc} >> R_L$ and that the intrinsic current gain, A_i = -1.) (13pts)



$i_{out}/i_s = \frac{R_S}{R_S + \frac{1}{g_m}}$

$g_m = \frac{I_C}{V_{th}}$

$\frac{R_S}{R_S + \frac{1}{g_m}} \geq 0.99$

$\Rightarrow R_S / \frac{1}{g_m} \geq \frac{0.99}{0.01} = 99$

$g_m \geq \frac{99}{R_S} \Leftrightarrow I_C \geq \frac{99}{R_S} \cdot V_{th}$

$I_C \geq 49.5\ \mu A$

$R_{out} \approx g_m r_o \cdot (r_\pi \| R_S)$

$= \frac{I_C}{V_{th}} \cdot \frac{V_{An}}{I_C} \cdot (r_\pi \| R_S)$

$= \frac{25}{25m} (r_\pi \| R_S) \geq 20\ M\Omega$

$\Rightarrow r_\pi \| R_S \geq 20\ k \Rightarrow r_\pi \geq \frac{100}{3}\ k\Omega$

$\frac{100}{I_C} \cdot 25m \geq \frac{100}{3}\ k$

$I_C \leq 75\ \mu A$

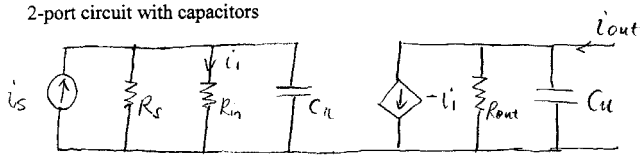
Design results $r_\pi = \frac{\beta_o}{g_m} = \frac{\beta_o V_{th}}{I_C}$

	expression	value	
I_{SUP} =	$\frac{99}{R_S} \cdot V_{th}$	49.5 uA	(75 uA)
I_{BIAS} =	$\frac{99}{R_S} \cdot V_{th}$	49.5 uA	(75 uA)
i_{out}/i_s =	$R_S / (R_S + \frac{1}{g_m})$	0.99	(0.994)
R_{out} =	$g_m r_o (r_\pi \| R_S) \approx \frac{V_{An}}{V_{th}} (\frac{\beta_o \cdot V_{th}}{I_C} \| R_S)$	25 MΩ	(20 MΩ)
R_{in} =	$1/g_m$	505 Ω	(333 Ω) ↑ Alternative design

$r_\pi = 50.5K$ $R_{out} = \frac{25}{25m} \cdot (50.5K \| 50K) \approx 25\ M\Omega$

2.2 Write the 2-port model[3] of this amplifier, add the C_π and C_μ parasitic capacitances at the proper locations and calculate C_π (assume that V_{BC}=-2V). Then, assuming that R_L=0 (shorted) find the pole of this amplifier and draw the magnitude and phase Bode plot of the current gain i_{out}/i_s. (12 pts)

2-port circuit with capacitors



$R_{in} = 1/g_m$ $\quad R_{out} \sim g_m r_o (r_\pi \| R_S)$

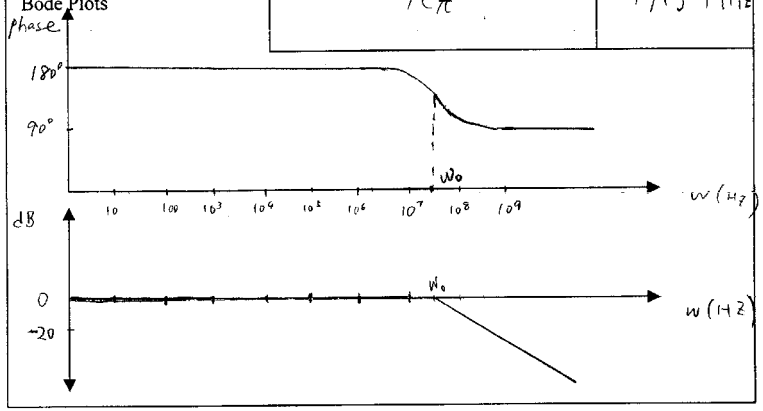
	expression	value
$C_\pi =$	$g_m \tau_F + C_{JE_0} = \frac{g_q}{R_S} \cdot 50p + \cdot 15f$	114 fF

Transfer function i_{out}/i_s as a function of ω.

$$\frac{i_{out}}{i_s} = -\frac{1/jwC_\pi}{R_{in} + 1/jwC_\pi} = -\frac{1}{1 + jwR_{in}C_\pi} = -\frac{1}{1 + jw\frac{C_\pi}{g_m}}$$

$\omega_0 =$ g_m/C_π $\quad$ 17.3 MHz

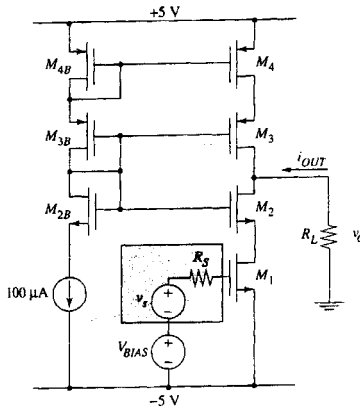
Bode Plots



[3] Please make sure that you draw the 2-port, and not the small signal model…

Problem 3 of 3: Answer each question briefly and clearly. (35 points)

3. Please do a complete analysis of this transconductance amplifier as follows. Make sure that you use the transistor parameters shown below.



$V_{Tp} = -0.7$ V
$\mu_p C_{ox} = 25\ \mu A/V^2$
$\lambda_p = 0.05\ V^{-1}$

$V_{Tn} = 0.7$ V
$\mu_n C_{ox} = 50\ \mu A/V^2$
$\lambda_n = 0.07\ V^{-1}$

$M_2 = M_{2B} = 40/1.5$
$M_3 = M_{3B} = 40/1.5$
$M_4 = M_{4B} = 40/1.5$

3.1 Calculate $(W/L)_1$ of M_1 such that the small-signal transconductance i_{out}/v_s = 1mS. Assume $R_L = 0\Omega$ for this part. (7pts)

$$g_{m_1} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = 1mS \Rightarrow$$

$$\frac{W}{L} = \frac{g_{m_1}^2}{2\mu_n C_{ox} I_D}$$

	expression	value
$(W/L)_1 =$	$\frac{g_{m_1}^2}{2\mu_n C_{ox} I_D}$ (g_{m_1} ← 1mS; I_D ← 100μA)	$100 = \frac{150}{1.5}$

3.2 Calculate the value of V_{BIAS} using the $(W/L)_1$ calculated in part a so that I_{OUT} = 0A. (7pts)

Iout cannot be 0A, since the output voltage cannot go as low as zero (M_2 would fall out of saturation!).

still, we should bias M_1 so that it draws 100μA in steady-state.

$I_D = \frac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{BIAS} - V_{Tn})^2 = 100\mu A$

	expression	value
V_{BIAS} =	$V_{Tn} + \sqrt{\frac{2I_D}{\frac{W}{L}\mu_n C_{ox}}}$	0.9V

3.3 Calculate the output resistance of this amplifier. (7pts)

$R_o = R_{up} \,//\, R_{down}$

$R_{up} = r_{o3} + r_{o4} + g_{m3} r_{o3} r_{o4} = 15M$

$R_{down} = r_{o2} + r_{o1} + g_{m2} r_{o1} r_{o2} = 10.6M$

	expression	value
Rout =	$(r_{o1} + r_{o4} + g_{m3} r_{o3} r_{o4}) \,//\, (r_{o2} + r_{o1} + g_{m2} r_{o1} r_{o2})$	6.23MΩ

3.4 Find the maximum and the minimum value of the output voltage, and state which transistor limits it in each case, when unloaded (R_L=infinity) (7pts)

$V_{GS4} = V_{G3} = V_T + \sqrt{\frac{I_D}{\frac{1}{2}\mu_p C_{ox}\frac{W}{L}}} = 1.24V$

	expression	value
V_{out} max =	$V_{G3} - V_{Tn}$	3.22V
limited by:	M_3, whose gate is at 7.52V	
V_{out} min =	$V_{G2} - V_{Tn}$	1.82V
limited by:	M_2, whose gate is at 7.52V	

3.5 What is the maximum value of the load resistor R_L at which the overall transconductance is degraded by 20% from the original value of 1mS? (7pts)

$G_M = g_{m1}\frac{R_{out}}{R_{out} + R_L} = g_{m1} \cdot 0.8$

$\frac{R_{out}}{R_{out} + R_L} = 0.8 \Rightarrow \frac{R_{out}}{0.8} = R_{out} = R_{L\,max}$

	expression	value
$R_{L\,max}$ =	$R_{out}\left(\frac{1}{0.8} - 1\right)$	1.56MΩ