Name **[1 point]**: _____**AMIN**_____

SID: _____

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Midterm 1	**EECS 105**
B. E. BOSER	**September 28, 2004**	**FALL 2004**

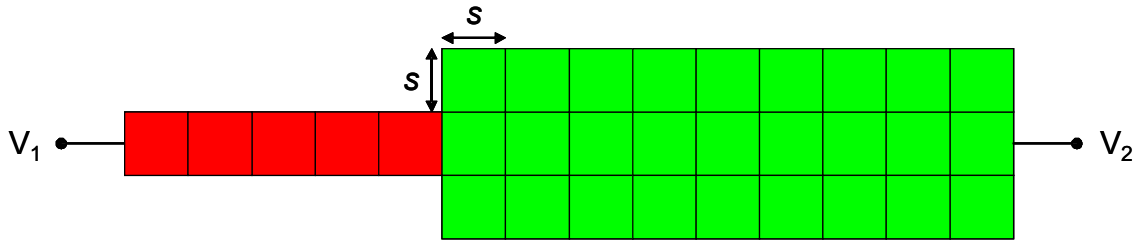
*Show derivations and **mark results** with box around them. Erase or cross out erroneous attempts. Simplify algebraic results as much as possible! Mark your name and SID at the top of the exam and all extra sheets.*

For Office Use Only:

	Points
Problem 1	/25
Problem 2	/25
Problem 3	/24
Problem 4	/25
TOTAL	/100

Problem 1 [25 points]: Sheet resistance

Shown below is the layout of a p-type resistor with $N_A = 10^{17}$ cm^{-3}, $\mu_p = 250\,\mathrm{cm}^2/\mathrm{Vs}$ and thickness $t = 1$ μm. Electronic charge $q = 1.6\times10^{-19}\,\mathrm{C}$.



(a) [10 pts] Calculate the sheet resistance R_{sh} in Ω/ .

(b) [10 pts] Assuming $R_{sh} = 1\mathrm{k}\Omega/$ (not the correct answer for part a), calculate the resistance between terminals V_1 and V_2 for $s = 1\mu\mathrm{m}$.

(c) [5 pts] Repeat part (b) with $s = 2\mu\mathrm{m}$.

ANSWERS

(a) $$R_{sh} = \frac{1}{q \cdot p \cdot \mu_p \cdot t} = \frac{1}{q \cdot N_A \cdot \mu_p \cdot t} = \frac{1}{(1.6x10^{-19}\,C)\cdot(10^{17}\,cm^{-3})\cdot(250\,cm^2/Vs)\cdot(10^{-4}\,cm)}$$

$$\therefore R_{sh} = 2500\,\Omega/square$$

(b) The number of squares in the segment marked by red is $\frac{5s}{1s} = 5$. The number of squares in the segment marked by green is $\frac{9s}{3s} = 3$. Hence, the total number of squares equals $5 + 3 = 8$. As a result,

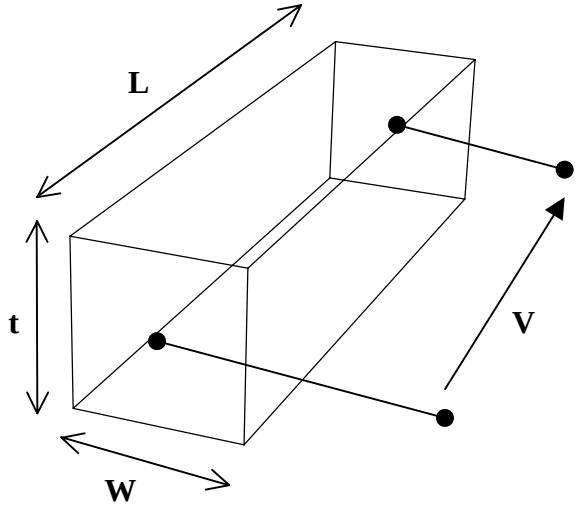
$$R = R_{sh} \cdot (number\ \ of\ \ squares) = (1\,k\Omega/square)\cdot(8\ \ squares) = 8k\Omega.$$

(c) From part (b), the value of s does not enter into the expression for R. Hence, the value for R is unaffected from part (b) and is equal to $8k\Omega$.

Problem 2 [25 points]: Carrier transport

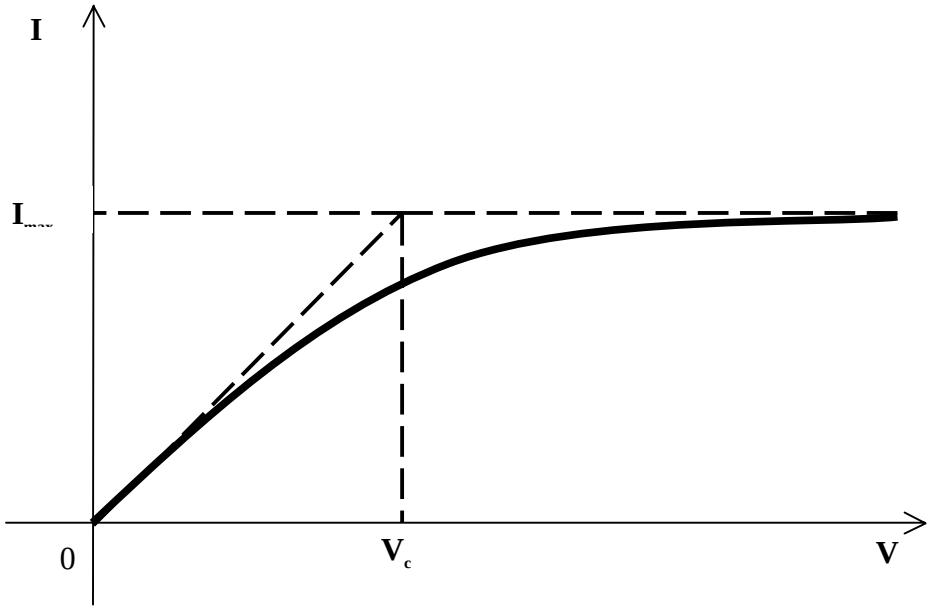
In this problem, you are to design an over-current protection device. Assume that the slab of silicon shown below is doped with an acceptor concentration of N_a (with $N_a >> n_i$).

$N_a = 10^{16}\ \text{cm}^{-3}$, $\mu_p = 250\ \text{cm}^2/\text{Vs}$, $v_{sat,p} = 10^6\ \text{cm/s}$, $t = 10\mu\text{m}$, $W = 50\ \mu\text{m}$, $L = 100\ \mu\text{m}$, electronic charge $q = 1.6\times10^{-19}\ \text{C}$.



(a) [15 pts] Derive an analytical expression and calculate the numerical value for the maximum current I_{max}.

(b) [10 pts] Derive an analytical expression and calculate the numerical value for V_c (see the I-V curve below for the definition of V_c).



ANSWERS

(a)
$$I_{\max} = q \cdot p \cdot v_{sat,p} \cdot A = q \cdot N_a \cdot v_{sat,p} \cdot W \cdot t$$
$$\therefore I_{\max} = (1.6x10^{-19}\,C) \cdot (10^{16}\,cm^{-3}) \cdot (10^{6}\,{cm}/{s}) \cdot (50x10^{-4}\,cm) \cdot (10x10^{-4}\,cm) = 8mA$$

(b)
$$v_{sat,p} = \mu_p \cdot E_c = \mu_p \cdot \frac{V_c}{L} \Rightarrow V_c = \frac{v_{sat,p} \cdot L}{\mu_p}$$
$$\therefore V_c = \frac{(10^{6}\,{cm}/{s}) \cdot (100x10^{-4}\,cm)}{250\,{cm^2}/{Vs}} = 40V$$

Problem 3 [24 points]: Region of operation

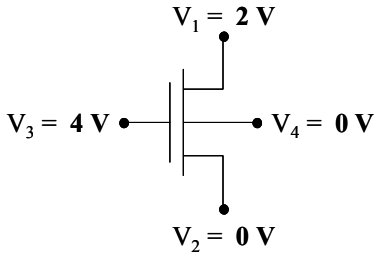
Shown below are both NMOS and PMOS transistors with various terminal voltages referred to ground. Identify the source terminal (V_1 or V_2) and the region of operation (cutoff or triode) of each transistor by circling the correct answer in the table provided.

NMOS	PMOS
V_{T0n} = **1** V	V_{T0p} = **-1** V
$_n$ = **1** V$^{1/2}$	$_p$ = **-1** V$^{1/2}$
$_p$ = **-0.5** V	$_n$ = **0.5** V

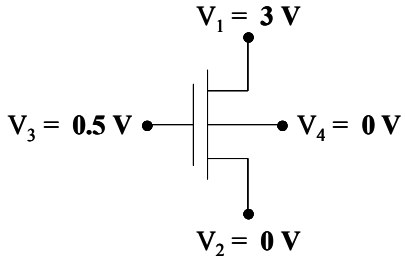
$$V_{Tn} = V_{T0n} + \gamma_n\left(\sqrt{-2\varphi_p - V_{BS}} - \sqrt{-2\varphi_p}\right)$$

$$V_{Tp} = V_{T0p} + \gamma_p\left(\sqrt{2\varphi_n - V_{SB}} - \sqrt{2\varphi_n}\right)$$

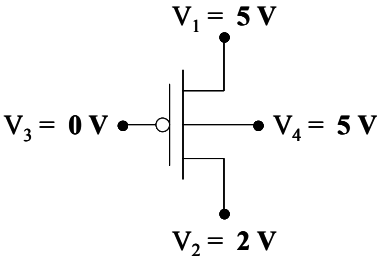
Example



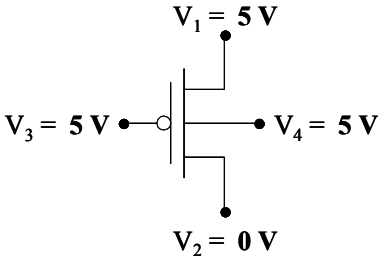
(a)



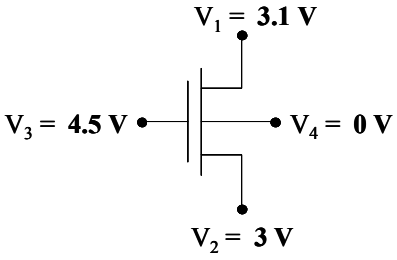
(b)



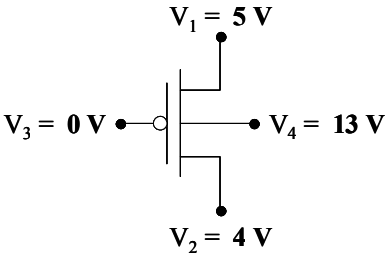
(c)



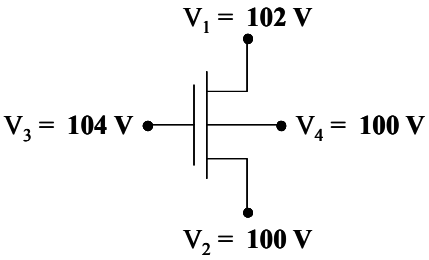
(d)



(e)



(f)



Circuit	Source Terminal		Region	
Example	V_1	(**V_2**)	Cutoff	(Triode)
(a)	V_1	V_2	Cutoff	Triode
(b)	V_1	V_2	Cutoff	Triode
(c)	V_1	V_2	Cutoff	Triode
(d)	V_1	V_2	Cutoff	Triode
(e)	V_1	V_2	Cutoff	Triode
(f)	V_1	V_2	Cutoff	Triode

ANSWERS

(a) V_2 is the **source** terminal. Also, $V_{Tn} = V_{Tn0} = 1V$ because the source (V_2) and bulk (V_4) are at the same potential. The NMOS transistor is **cutoff** because

$V_{GS} = V_3 - V_2 = 0.5V - 0V = 0.5V < V_{Tn} = 1V$.

(b) V_1 is the **source** terminal. Also, $V_{Tp} = V_{Tp0} = -1V$ because the source (V_1) and bulk (V_4) are at the same potential. The PMOS transistor is in **triode** because

$V_{SG} = V_1 - V_3 = 5V - 0V = 5V > |V_{Tp}| = 1V$

and

$V_{SD} = V_1 - V_2 = 5V - 2V = 3V < V_{SG} - |V_{Tp}| = V_1 - V_3 - |V_{Tp}| = 5V - 0V - 1V = 4V$.

(c) V_1 is the **source** terminal. Also, $V_{Tp} = V_{Tp0} = -1V$ because the source (V_1) and bulk (V_4) are at the same potential. The PMOS transistor is **cutoff** because

$V_{SG} = V_1 - V_3 = 5V - 5V = 0V < |V_{Tp}| = 1V$.

(d) V_2 is the **source** terminal. Also, V_4 is the bulk terminal. As a result,

$$V_{Tn} = V_{Tn0} + \gamma_n(\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p}) = V_{Tn0} + \gamma_n(\sqrt{-2\phi_p - (V_4 - V_2)} - \sqrt{-2\phi_p})$$
$$\therefore V_{Tn} = 1V + 1\sqrt{V} \cdot (\sqrt{1V - (-3V)} - \sqrt{1V}) = 2V$$

The NMOS transistor is **cutoff** because $V_{GS} = V_3 - V_2 = 4.5V - 3V = 1.5V < V_{Tn} = 2V$.

(e) V_1 is the **source** terminal. Also, V_4 is the bulk terminal. As a result,

$$V_{Tp} = V_{Tp0} + \gamma_p(\sqrt{2\phi_n - V_{SB}} - \sqrt{2\phi_n}) = V_{Tp0} + \gamma_p(\sqrt{2\phi_n - (V_1 - V_4)} - \sqrt{2\phi_n})$$
$$\therefore V_{Tp} = -1V + (-1\sqrt{V}) \cdot (\sqrt{1V - (-8V)} - \sqrt{1V}) = -3V$$

The PMOS transistor is in **triode** because

$V_{SG} = V_1 - V_3 = 5V - 0V = 5V > |V_{Tp}| = 3V$

and

$V_{SD} = V_1 - V_2 = 5V - 4V = 1V < V_{SG} - |V_{Tp}| = V_1 - V_3 - |V_{Tp}| = 5V - 0V - 3V = 2V$.

(f) V_2 is the **source** terminal. Also, $V_{Tn} = V_{Tn0} = 1V$ because the source (V_2) and bulk (V_4) are at the same potential. The NMOS transistor is in **triode** because

$$V_{GS} = V_3 - V_2 = 104V - 100V = 4V > V_{Tn} = 1V$$

and

$$V_{DS} = V_1 - V_2 = 102V - 100V = 2V < V_{GS} - V_{Tn} = V_3 - V_2 - V_{Tn} = 104V - 100V - 1V = 3V .$$

Problem 4 [25 points]: CMOS switch

For this problem, ignore the backgate effect; that is, let $\gamma_n = \gamma_p = 0$.

NMOS	PMOS
V_{T0n} = **1** V	V_{T0p} = **-1** V
$\mu_n C_{ox}$ = **200** μA/V²	$\mu_p C_{ox}$ = **100** μA/V²

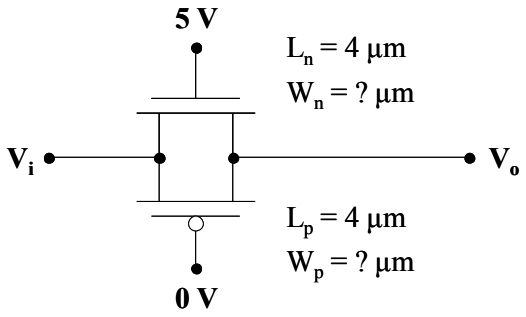


Figure 1: CMOS switch for part (a).

(a) [15 pts] Find W_n and W_p such that R_{io} = 1 kΩ for both $V_i = V_o$ = 0 V and $V_i = V_o$ = 5 V (see Figure 1 above). R_{io} is the resistance between the input and output terminals, V_i and V_o.

(b) [10 pts] Now, let W_n = 10 μm and W_p = 40 μm (see Figure 2 below). NOTE: these are <u>not</u> the answers you found for part (a). Calculate R_{io} for $V_i = V_o$ = 2 V.

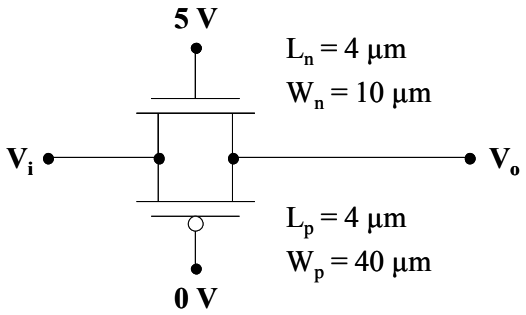


Figure 2: CMOS switch for part (b).

ANSWERS

For $V_{DS} = 0$, $R_{NMOS} = \dfrac{1}{\mu_n C_{ox} \cdot (\dfrac{W}{L})_n \cdot (V_{GS} - V_{Tn0})}$ (1).

Also, for $V_{SD} = 0$, $R_{PMOS} = \dfrac{1}{\mu_p C_{ox} \cdot (\dfrac{W}{L})_p \cdot (V_{SG} - |V_{Tp0}|)}$ (2).

(a) For $V_i = V_o = 0V$, the PMOS transistor is off. Hence,

$R_{io} = R_{NMOS} = \dfrac{1}{(200 \mu A/V^2) \cdot (\dfrac{W}{4\mu m})_n \cdot (5V - 0V - 1V)} = 1k\Omega$. Solving for W_n yields,

$W_n = 5\mu m$.

For $V_i = V_o = 5V$, the NMOS transistor is off. Hence,

$R_{io} = R_{PMOS} = \dfrac{1}{(100 \mu A/V^2) \cdot (\dfrac{W}{4\mu m})_p \cdot (5V - 0V - 1V)} = 1k\Omega$. Solving for W_p yields,

$W_p = 10\mu m$.

(b) From (1) above, $R_{NMOS} = \dfrac{1}{(200 \mu A/V^2) \cdot (\dfrac{10\mu m}{4\mu m}) \cdot (5V - 2V - 1V)} = 1k\Omega$. Similarly,

using (2) above, $R_{PMOS} = \dfrac{1}{(100 \mu A/V^2) \cdot (\dfrac{40\mu m}{4\mu m})_p \cdot (2V - 0V - 1V)} = 1k\Omega$. But, R_{io} is the

parallel combination of R_{NMOS} and R_{PMOS}. Hence,

$R_{io} = \dfrac{R_{NMOS} \cdot R_{PMOS}}{R_{NMOS} + R_{PMOS}} = 500\Omega$.