UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits — Fall 2007

MIDTERM EXAMINATION #2
Time allotted: 80 minutes

NAME: SOLUTIONS _____ _____
(print) Last First Signature

STUDENT ID#: _____

INSTRUCTIONS:
1. **Use the values of physical constants provided below.**
2. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
3. **Clearly mark (underline or box) your answers.**
4. **Specify the units on answers whenever appropriate.**

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

Note that $V_T \ln(10) = 0.060$ V at T=300K

PROPERTIES OF SILICON AT 300K

Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

SCORE:

1 _____ **/ 10**

2 _____ **/ 15**

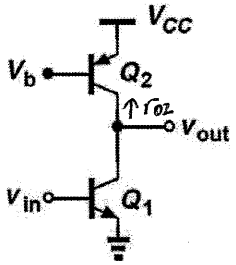
3 _____ **/ 25**

4 _____ **/ 30**

Total: _____ **/ 80**

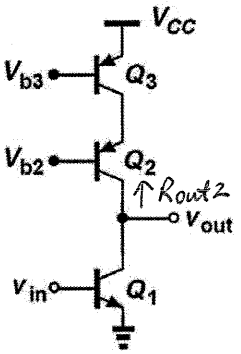
Problem 1 [10 points]: Cascode Stages

a) Consider the common-emitter amplifier stage below. What is the benefit of using a PNP BJT (rather than a resistor) as the load device? **[2 pts]**



The PNP BJT provides a large load resistance (r_{O2}) (beneficial for achieving large voltage gain) without requiring a large voltage drop ($\sim 0.4V \ll I_C r_O$) and therefore provides for more headroom than a resistor.

b) Explain qualitatively why the voltage gain of this stage is improved by using a PNP cascode as shown below. Derive a simplified expression for the voltage gain in terms of the BJT small-signal parameters (g_{m1}, $r_{\pi 1}$, r_{o1}, *etc.*). **[5 pts]** You may assume that $\beta = g_m r_\pi >> 1$ and that $r_\pi << r_o$ for each of the transistors.



The load resistance (seen looking into the collector of Q_2) is enhanced by using a PNP cascode as the load.

$$R_{out2} \simeq g_{m2} r_{O2} (r_{O3} \| r_{\pi 2}) >> r_{O2}$$

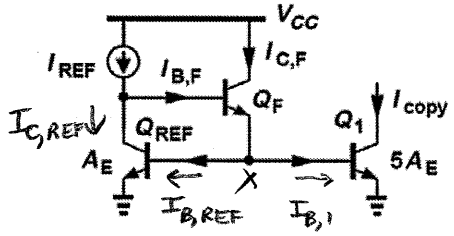
$$A_V = -g_{m1} (r_{O1} \| R_{out2}) = -g_{m1} [r_{O1} \| (g_{m2} r_{O2} (r_{O3} \| r_{\pi 2}))]$$

$$\simeq -g_{m1} (r_{O1} \| \beta r_{O2})$$

c) Qualitatively, how should the values of the base bias voltages (V_{b2} and V_{b3}) for the PNP transistors be selected? **[3 pts]**

- V_{b3} should be selected so that V_{EB} yields the required DC bias current ($I_C = I_S \exp\left(\frac{V_{EB}}{V_T}\right)$).
- V_{b2} should be selected as the highest voltage that guarantees that Q_2 and Q_3 are each operating in the active region (to provide a large load resistance).

Problem 2 [15 points]: Current Mirrors
Consider the circuit shown below:



The BJTs are of identical design, except for their emitter areas:
- The emitter area of Q_F is equal to the emitter area of Q_{REF}
- The emitter area of Q_1 is 5 times larger than the emitter area of Q_{REF}

a) What is the purpose of the transistor Q_F? **[3 pts]**

Q_F supplies the base currents for Q_{REF} and Q_1, without drawing much current from the current source (I_{REF}) so that $I_{C,REF} \simeq I_{REF}$.

b) Derive an expression for I_{copy} in terms of I_{REF}, neglecting the effect of the transistor base currents. **[4 pts]**

Noting that the base-emitter voltages are the same for Q_{REF} and Q_1:

$$V_X = V_T \ln\left(\frac{I_{C,REF}}{I_{S,REF}}\right) = V_T \ln\left(\frac{I_{copy}}{I_{S,1}}\right)$$

$$\Rightarrow \frac{I_{C,REF}}{I_{S,REF}} = \frac{I_{copy}}{I_{S,1}} \quad \Rightarrow \quad I_{copy} = \frac{I_{S,1}}{I_{S,REF}}(I_{C,REF}) \simeq \frac{I_{S,1}}{I_{S,REF}}(I_{REF})$$

I_S is proportional to emitter area, so $\frac{I_{S,1}}{I_{S,REF}} = \frac{5A_E}{A_E} = 5$. $\therefore$ $I_{copy} = 5I_{REF}$

c) Considering the effect of the transistor base currents, what is the error in I_{copy}? **[8 pts]**
Assume that β is the same for all transistors, and that it is large (so that $I_E \cong I_C$ for each transistor).

$$I_{B,REF} = \frac{I_{C,REF}}{\beta} = \frac{I_{copy}/5}{\beta} \qquad I_{B,1} = \frac{I_{copy}}{\beta} \qquad I_{C,F} \simeq I_{E,F} = I_{B,REF} + I_{B,1}$$

KCL at collector of Q_{REF}: $I_{REF} = I_{C,REF} + I_{B,F} = I_{C,REF} + \frac{I_{C,F}}{\beta}$

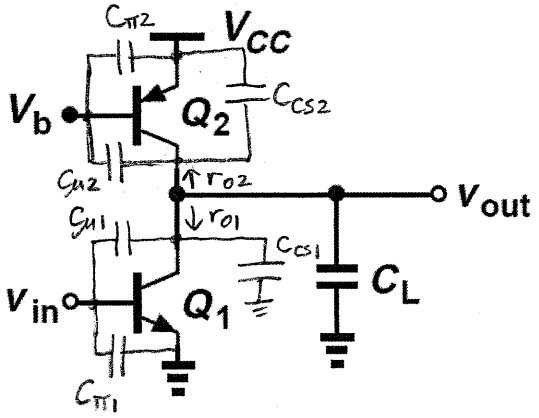
$$\Rightarrow I_{REF} = \frac{I_{copy}}{5} + \frac{1}{\beta}\left[\frac{I_{copy}/5}{\beta} + \frac{I_{copy}}{\beta}\right] = I_{copy}\left\{\frac{1}{5} + \frac{1}{5\beta^2} + \frac{1}{\beta^2}\right\}$$

$$I_{copy} = \frac{I_{REF}}{\frac{1}{5} + \frac{1}{5\beta^2} + \frac{1}{\beta^2}} = \frac{5I_{REF}}{1 + \frac{1}{\beta^2} + \frac{5}{\beta^2}} = \frac{5I_{REF}}{1 + \frac{6}{\beta^2}} \simeq 5I_{REF}\left(1 - \frac{6}{\beta^2}\right)$$

$\therefore$ The fractional error in I_{copy} is $\boxed{\frac{-6}{\beta^2}}$

Problem 3 [25 points]: Frequency Response

Consider the amplifier stage shown below. Assume that $V_A \neq \infty$ for each transistor, and that each transistor is DC-biased to operate in the active mode.



a) Derive an expression for the low-frequency voltage gain. **[4 pts]** This is a common-emitter stage. The load resistance (seen looking into the collector of Q_2) is r_{O2}, which is in parallel (between the output node and AC ground) with r_{O1}.

$$A_{v0} = -g_{m1}(r_{O1} \| r_{O2})$$

b) Why is it desirable to minimize the capacitive load (C_L)? **[3 pts]**

The load capacitance results in a pole in the transfer function, i.e. causes the voltage gain to decrease when the signal frequency increases above the pole frequency $\propto \frac{1}{C}$. Small C_L is desirable to increase the pole frequency, for large bandwidth.

c) Draw the BJT junction capacitances ($C_{\pi 1}$, $C_{\mu 1}$, C_{CS1}, $C_{\pi 2}$, $C_{\mu 2}$, C_{CS2}) on the circuit diagram above. **[6 pts]** (Note: The substrate of a PNP BJT is n-type, and so it is biased at V_{CC} to ensure that the collector-substrate junction is never forward-biased.)

d) Use Miller's theorem to derive an approximate expression for the -3dB bandwidth. Assume that the dominant pole is associated with the output node. **[8 pts]**

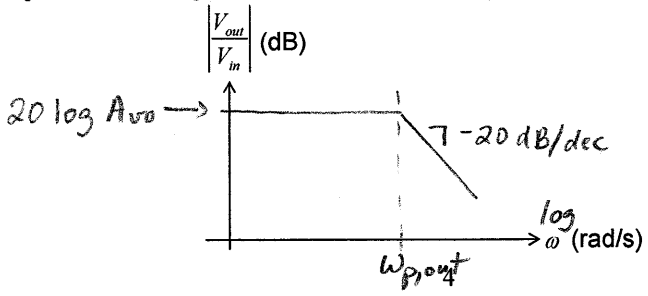
$C_{\mu 1}$ contributes an effective capacitance between the output node and ground, of value $\left(1 - \frac{1}{A_{v0}}\right) C_{\mu 1} = \left(1 + \frac{1}{g_{m1}(r_{O1} \| r_{O2})}\right) \simeq C_{\mu 1}$.

This is in parallel with the capacitances $C_{\mu 2}$, C_{CS2}, C_{CS1}, and C_L.

The -3dB bandwidth is the frequency of the pole associated with the output node:

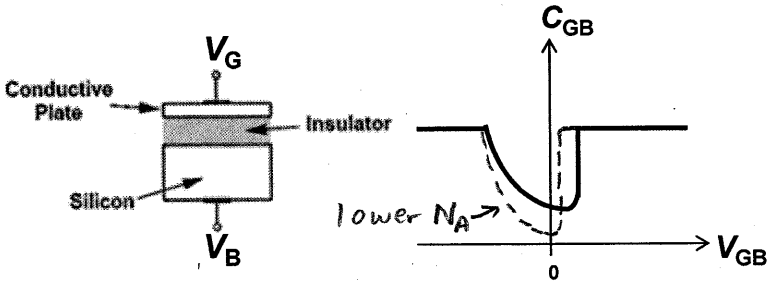
$$BW = \omega_{p,out} = \left[(r_{O1} \| r_{O2})(C_{\mu 1} + C_{\mu 2} + C_{CS1} + C_{CS2} + C_L)\right]^{-1} \text{ rad/s}$$

e) Sketch the Bode plot on the axes provided. Label the low-frequency voltage gain and -3dB bandwidth. **[4 pts]**



Problem 4 [30 points]: MOS Devices

a) Shown below is the capacitance-*vs.*-voltage (*C-V*) characteristic for an MOS capacitor.



i) Is the silicon n-type or p-type? **[1 pt]**

This is an NMOS device.

ii) Indicate **by drawing a dashed line** how the *C-V* curve would change if the **Si dopant concentration were to be reduced.** (Assume that the flatband voltage does not change significantly.) **[4 pts]**

- V_{TH} ↓
- C_{min} ↓
- $C_{max} = C_{ox}$ stays the same

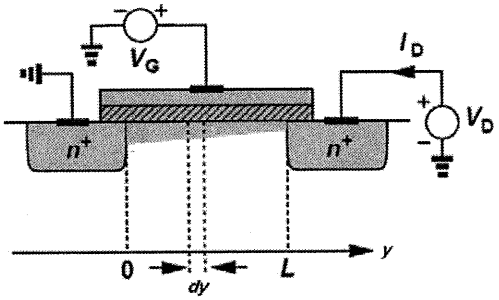
b) Explain why the current in a **long-channel MOSFET** does not depend on the drain-to-source voltage (V_{DS}), when the MOSFET is operating in the saturation region. **[5 pts]**

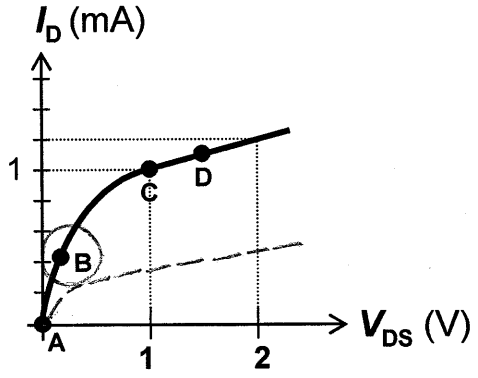
In the saturation region of operation, the inversion layer is "pinched off" near the drain. As V_{DS} is increased, the voltage dropped across the pinch-off region increases, while the voltage dropped across the inversion does not change (staying constant at $V_{GS}-V_{TH}$). Thus, the lateral electric field in the inversion layer does not increase, so that the carrier velocity does not increase, hence current does not change.

c) Indicate in the table below (by checking the appropriate box) how the parameters for a **short-channel MOSFET** would change, if the **body dopant concentration were to be increased** (*e.g.* by a factor of 10). Justify your answers. **[9 pts]**

MOSFET Parameter	Parameter will			Brief Justification (Qualitative reasoning)
	increase	decrease	not change	
Body effect parameter, γ	✓			Capacitive coupling between the channel potential and the body voltage is increased, since C_{dep} ↗
Transconductance, g_m			✓	g_m is only dependent on W, v_{sat}, and t_{ox} for a short-channel MOSFET, None of these are affected by the body dopant concentration.
Output resistance, r_o	✓			The widths of the source/drain junction depletion regions will decrease, so that these junctions support a smaller fraction of the depletion charge underneath the gate. ∴ Drain-induced barrier lowering (decreasing V_{TH} with increasing V_{DS}) is reduced.

d) Consider a **long-channel** MOSFET of channel length L, whose cross-section is shown below. Assume that $V_S = V_B = 0$.





i) Identify the MOSFET operating point on the *I-V* characteristic to the right. (Circle the appropriate letter.) Briefly justify your answer. **[2 pts]**

An inversion layer exists across the entire length of the channel, so that the current depends on both V_{DS} and V_{GS}.

$\Rightarrow$ Triode region of operation

ii) If the threshold voltage (V_{TH}) is 0.5 V, what is the gate-to-source bias, V_{GS}? **[2 pts]**

The saturation voltage is 1V (from the plot).

$\Rightarrow V_{GS} - V_{TH} = 1V$

$V_{GS} = V_{TH} + 1V = \boxed{1.5V}$

iii) Estimate the numerical value of the channel length modulation coefficient, λ **[4 pts]** $I_D = I_{D0}[1 + \lambda(V_{DS} - V_{Dsat})]$

From the plot, I_D increases from 1mA to 1.2 mA (i.e. by 20%) in the saturation region, when V_{DS} increases from 1V to 2V.

$\lambda(V_{DS} - V_{Dsat}) = 0.2 \quad \Rightarrow \boxed{\lambda = 0.2\ V^{-1}}$

iv) Indicate **by drawing a dashed curve on the plot above** how the *I-V* characteristic would change, if the gate bias were to be decreased such that V_{GS}-V_{TH} **is reduced by a factor of 2. [3 pts]**

$V_{GS} - V_{TH}$ reduced by a factor of 2:

- V_{Dsat} reduced by a factor of 2
- I_{Dsat} reduced by a factor of 4
- λ is unchanged.