UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits — Fall 2008

MIDTERM EXAMINATION #2
Time allotted: 80 minutes

NAME: SOLUTIONS
(print) Last First Signature

STUDENT ID#:

INSTRUCTIONS:

1. **Use the values of physical constants provided below.**
2. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
3. **Clearly mark (underline or box) your answers.**
4. **Specify the units on answers whenever appropriate.**

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

Note that $V_T \ln(10) = 0.060$ V at T=300K

PROPERTIES OF SILICON AT 300K

Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

SCORE:

1 ________ / 15

2 ________ / 15

3 ________ / 20

4 ________ / 15

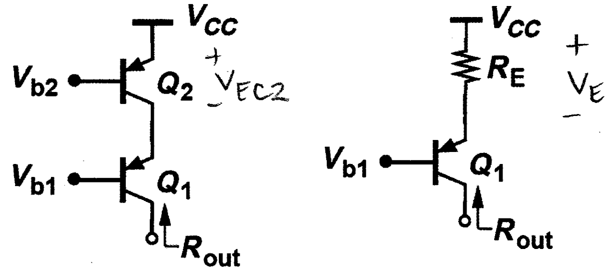
5 ________ / 15

Total: ________ / 80

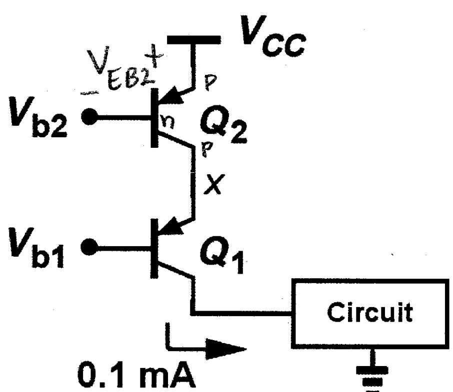
Problem 1 [15 points]: Cascodes

a) What is the advantage of using a BJT (Q_2, as shown below on the left) rather than a resistor (R_E, as shown below on the right) to achieve a high value of output resistance (R_{out})? **[3 pts]**

Q_2 provides a large degeneration resistance ($\sim r_{o2}$) without sustaining a large voltage drop (V_{EC2}) as compared with R_E for which the voltage drop $V_E \simeq I_{C1} R_E$ can be large if R_E is large. Thus, the use of a BJT rather than a resistor provides for larger headroom for the output voltage signal to swing.



b) Suppose a PNP cascode is to be used as a 0.1mA current source, as shown below. What should be the values of the bias voltages V_{b1} and V_{b2}? Assume that $\boldsymbol{I_S = 10^{-16}}$**A** for each BJT, and that the **$\boldsymbol{Q_2}$ collector junction is forward-biased by no more than 0.3V** to ensure that Q_2 operates in active mode. $\boldsymbol{V_{CC} = 2.5}$**V**. Note that $e^{0.72/0.026} \cong 10^{12}$. **[8 pts]**



In order for $I_{C1} \simeq I_{C2} = 0.1\,mA = 10^{-4}A$,

$|V_{BE}|$ for each BJT should be $V_T \ln\left(\frac{I_C}{I_S}\right)$:

$|V_{BE}| = 0.026 \ln\left(\frac{10^{-4}}{10^{-16}}\right) = 0.026 \ln 10^{12} = 12 \times 0.060 = 0.72V$

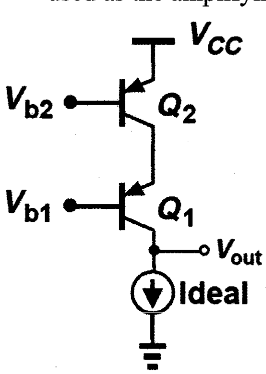
$V_{b2} = V_{CC} - V_{EB2} = 2.5V - 0.72V = \boxed{1.78V}$

If the Q_2 collector junction is forward-biased by 0.3V,

$V_X - V_{b2} = 0.3V \Rightarrow V_X = 0.3V + 1.78V = 2.08V$

$V_{b1} \leq V_X - V_{EB1} = 2.08V - 0.72V = \boxed{1.36V}$

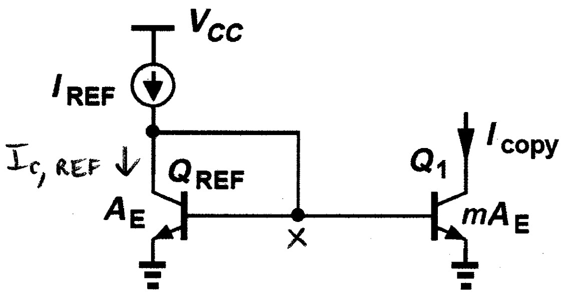
c) Suppose that a PNP cascode is to be used as a voltage amplifier, as shown below. Which transistor (Q_1 or Q_2) should be used as the amplifying device? Explain briefly. **[4 pts]**



Q_2 should be used as the amplifying transistor.

If the input voltage signal is applied to the base of Q_1, the voltage gain is not as high, due to emitter degeneration.

Problem 2 [15 points]: Current Mirrors
Consider the circuit shown below:



a) What is the purpose of the transistor Q_{REF}? **[2 pts]**

Q_{REF} generates a bias voltage for the base of the current-mirror transistor Q_1.

b) Derive an expression for I_{copy} in terms of I_{REF} and m, **neglecting the effect of the transistor base currents.** **[3 pts]**

Assuming that $I_{C,REF} = I_{REF}$, $V_X = V_T \ln\left(\frac{I_{REF}}{I_{S,REF}}\right) = V_T \ln\left(\frac{I_{copy}}{I_{S,1}}\right)$

$$\Rightarrow \frac{I_{REF}}{I_{S,REF}} = \frac{I_{copy}}{I_{S,1}} \Rightarrow I_{copy} = \frac{I_{S,1}}{I_{S,REF}} I_{copy}$$

I_S for a BJT is proportional to the emitter area. $\Rightarrow \frac{I_{S,1}}{I_{S,REF}} = \frac{mA_E}{A_E} = m$

$$\Rightarrow \boxed{I_{copy} = mI_{REF}}$$

c) **Considering the effect of the transistor base currents**, what is the error in I_{copy}? **[8 pts]**

Q_{REF} base current is $\frac{I_{C,REF}}{\beta} = \frac{I_{copy}}{m\beta}$; Q_1 base current is $\frac{I_{copy}}{\beta}$

Applying KCL: $I_{REF} = I_{C,REF} + \frac{I_{C,REF}}{\beta} + \frac{I_{copy}}{\beta} = \frac{I_{copy}}{m} + \frac{I_{copy}}{m\beta} + \frac{I_{copy}}{\beta}$

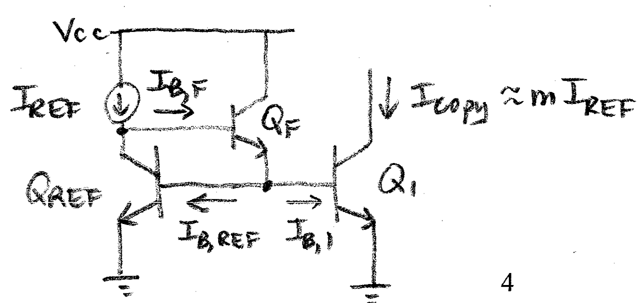
$$I_{REF} = I_{copy}\left[\frac{1}{m} + \frac{1}{m\beta} + \frac{1}{\beta}\right] = \frac{I_{copy}}{m}\left[1 + \frac{1}{\beta} + \frac{m}{\beta}\right]$$

$$I_{copy} = mI_{REF}\frac{1}{\left[1 + \frac{m+1}{\beta}\right]} \simeq mI_{REF}\left(1 - \frac{m+1}{\beta}\right)$$

$\Rightarrow$ fractional error is $\boxed{-\frac{m+1}{\beta}}$

d) How can the error in I_{copy} be reduced, without changing I_{REF}? **[2 pts]**

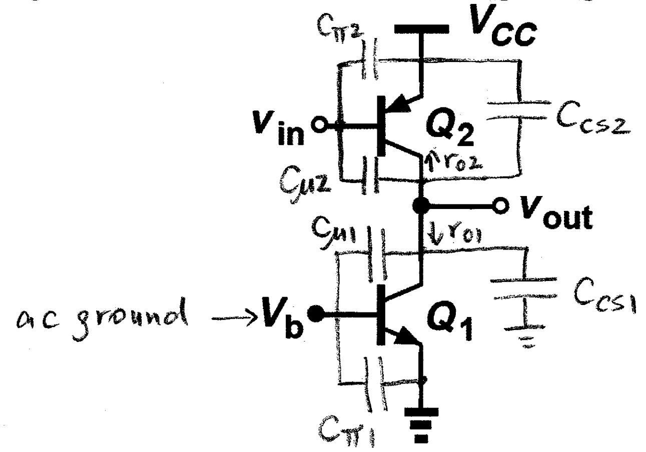
The error in I_{copy} can be reduced by using another transistor to supply the base currents for Q_{REF} and Q_1:



In this case, the fractional error is reduced by the factor β, since $I_{B,F} \simeq \frac{1}{\beta}(I_{B,REF} + I_{B,1})$.

Problem 3 [20 points]: Frequency Response

Consider the amplifier stage shown below. **Assume that $V_A \neq \infty$ for Q_1 and Q_2.**



a) Write an expression for the low-frequency voltage gain. **[4 pts]**

This is a common-emitter stage with "R_C" $= r_{o1} \| r_{o2}$:

$$\boxed{A_v = -g_{m2}(r_{o1} \| r_{o2})}$$

b) Why is the voltage gain of this amplifier dependent on the signal frequency? **[2 pts]**

The BJTs have junction capacitances, whose impedances depend on the signal frequency.

c) Draw the BJT junction capacitances ($C_{\pi 1}$, $C_{\mu 1}$, C_{CS1}, $C_{\pi 2}$, $C_{\mu 2}$, C_{CS2}) on the circuit diagram above. **[6 pts]**

d) Use Miller's theorem to derive an expression for the bandwidth. Assume that the dominant pole is associated with the **input node. [6 pts]**

The floating capacitance $C_{\mu 2}$ can be converted into a grounded capacitance at the input node $C_{\mu 2}(1-A_v)$.

The total capacitance seen at the input node is $C_{\pi 2} + C_{\mu 2}(1-A_v)$.

The resistance seen at the input node is $r_{\pi 2}$.

The pole associated with the input node is $\omega_{p,in} = \dfrac{1}{r_{\pi 2}[C_{\pi 2} + C_{\mu 2}(1-A_v)]}$ which is the bandwidth (in units of rad/s)

e) Considering your answers to parts **(a)** and **(d)** above, describe the trade-off between voltage gain and bandwidth. **[2 pts]**

In order to achieve large voltage gain, g_{m2} should be large.

If g_{m2} is large, then $r_{\pi 2} = \dfrac{\beta}{g_{m2}}$ is small $\Rightarrow$ bandwidth will be large.

$\Rightarrow$ There is no trade-off between A_v and BW.

(Actually, $\omega_{p,in}$ will not be the dominant pole anymore.)

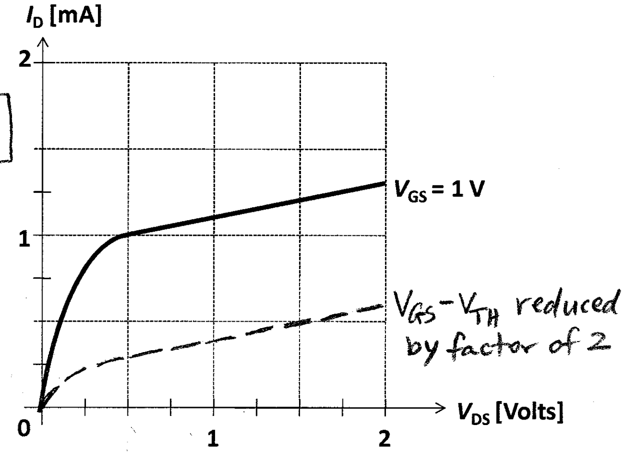
Problem 4 [15 points]: MOSFETs

a) Consider a long-channel MOSFET with the *I-V* characteristic as shown below.

i) What is the threshold voltage (V_{TH}) of this device? **[2 pts]**

From the plot, $V_{Dsat} = 0.5V$.

$V_{Dsat} = V_{GS} - V_{TH} \Rightarrow V_{TH} = V_{GS} - V_{Dsat} = \boxed{0.5V}$



ii) Indicate (by drawing a **dashed curve** on the plot) how the *I-V* characteristic would change if V_{GS}-V_{TH} were to be decreased by a factor of 2. **[3 pts]**

V_{Dsat} decreases by 2X

$I_{Dsat} \propto (V_{GS} - V_{TH})^2$ decreases by 4X

λ is unchanged

b) Indicate how the small-signal parameters of a **long-channel MOSFET** would change, if the **gate-oxide thickness were to be decreased.** Assume V_{GS}-V_{TH} remains the same. Give **qualitative explanations** for your answers. **[6 pts]**

MOSFET Parameter	Parameter will (check one) increase	decrease	not change	Brief Justification
Transconductance, g_m	✓			Capacitive coupling of the channel potential to the gate voltage is increased, so V_G will have a stronger influence on I_D
Output resistance, r_o		✓		The channel-length modulation effect is not affected by tox, i.e. λ does not change. However, I_D increases if tox increases (for the same reason as above) and so $r_o \approx \frac{1}{\lambda I_D}$ decreases.

c) What is the channel length modulation effect? **[2 pts]**

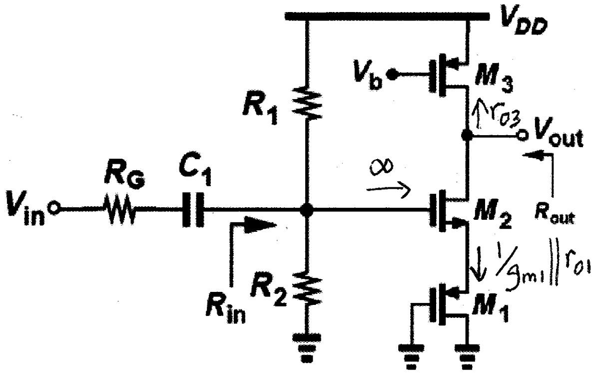
The drain current increases with increasing V_{DS} in the saturation region of operation, due to the length of the inversion-layer channel decreasing.

e) Why does the drain current eventually saturate in a **short-channel MOSFET**, as the drain-to-source voltage (V_{DS}) is increased? **[2 pts]**

The drain current in a short-channel MOSFET eventually saturates as V_{DS} increases, due to velocity saturation.

Problem 5 [15 points]: MOSFET Amplifiers Assume that $\frac{1}{g_m} \ll r_o$ for each MOSFET

Consider the MOSFET amplifier stage shown below. Assume that $\lambda \neq 0$ for each of the long-channel MOSFETs.



a) What type of amplifier is this **[2 pts]**? Circle one of the following, and **justify your answer**:

Common Emitter **Common Base** **Follower** **Cascode**

Input signal is applied to gate of M_2.
Output signal is taken from drain of M_2.

b) What is the purpose of transistor M_3? **[2 pts]**

M_3 serves as a current source.

c) What is the purpose of the capacitor C_1? **[2 pts]**

C_1 is used to couple the input voltage signal to the gate of the amplifying transistor (M_2), without affecting the DC bias.

d) Derive expressions for the low-frequency voltage gain (A_v), input resistance (R_{in}), and output resistance (R_{out}). **[9 pts]**

The resistance seen looking into the drain of M_2 is approximately

$$g_{m2} r_{02} \cdot \left(\frac{1}{g_{m1}} \| r_{01}\right)$$

so the total resistance seen looking into the output node is

$$R_{out} = r_{03} \| g_{m2} r_{02} \left(\frac{1}{g_{m1}} \| r_{01}\right) \approx r_{03} \| r_{02}$$ since $g_{m1} \approx g_{m2}$ (since $I_{D1} = I_{D2}$)

Since the resistance looking into the gate of M_2 is infinite,

$$R_{in} = R_1 \| R_2$$

$$A_v \cong \frac{R_1 \| R_2}{R_G + R_1 \| R_2} \cdot \frac{-r_{03}}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$