UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 105: Microelectronic Devices and Circuits — Fall 2009

MIDTERM EXAMINATION #2
10/29/2009
Time allotted: 75 minutes

NAME: ______________________ ______________________

STUDENT ID#: __________________

INSTRUCTIONS:

1. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
2. **Clearly mark (underline or box) your answers.**
3. **Specify the units on answers whenever appropriate.**
4. **Unless specified otherwise, include EARLY effect in your analysis.**

SCORE: 1	_________	**/ 16**
2	_________	**/ 16**
3	_________	**/ 18**
Total	_________	**/ 50**

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

PROPERTIES OF SILICON AT 300K

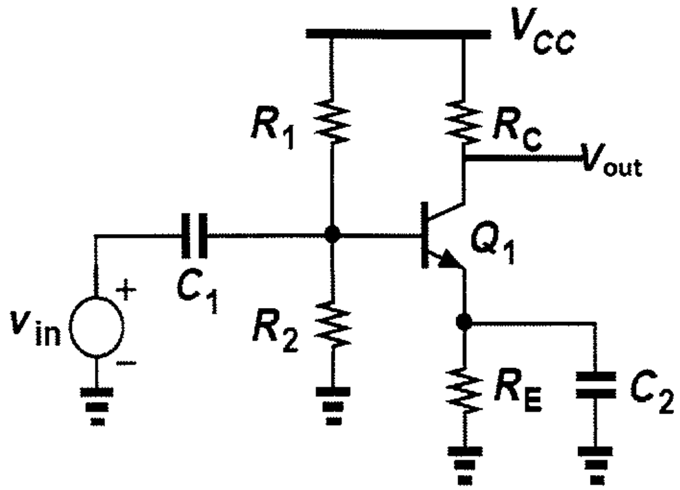
Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

USEFUL NUMBERS

V_T ln(10) = 0.060 V at T=300K
exp(30) ~ 10^{13}

Problem 1: BJT Amplifiers [16 pts]

Consider the BJT amplifier shown below. Ignore Early effect for all cases.



a) [2 pts] How does R_1 and R_2 help the amplifier?

to minimize β variation

b) [2 pts] What is the purpose of having R_E?

minimize the effect of variation in R_1 and R_2.

c) [6 pt] What are the input and output resistances?

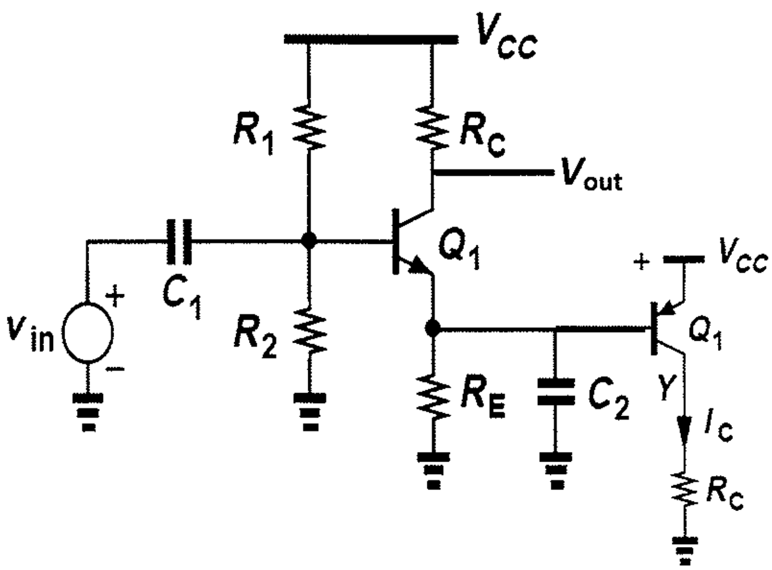
$Z_{in} = R_1 \| R_2 \| r_\pi$

$Z_{out} = R_C$

d) [3 pts] What is the small signal voltage gain?

$$A_V = -\frac{R_C}{1/g_m} = -g_m R_C$$

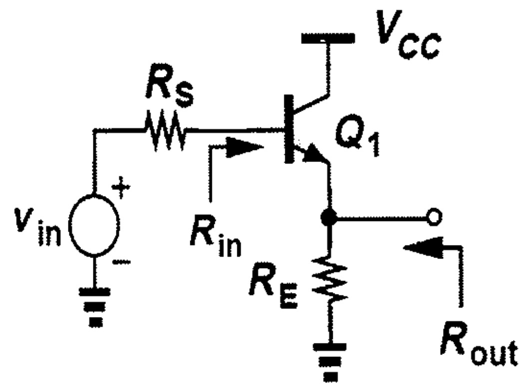
e) [3 pts]Now consider that a PNP transistor is added to the emitter of the amplifier as shown below. What will be the small signal voltage gain?



$A_V = -g_m R_C$ because PNP transistor is shorted by C_2.

PROB 2. BJT Amplifiers and Cascodes [16 pts].

a) [6 pts] What is the gain of the following amplifier? Where would you use such an amplifier? Why? Ignore the early effect.



$$A_v = \frac{R_E}{1/g_m + R_E} < 1$$

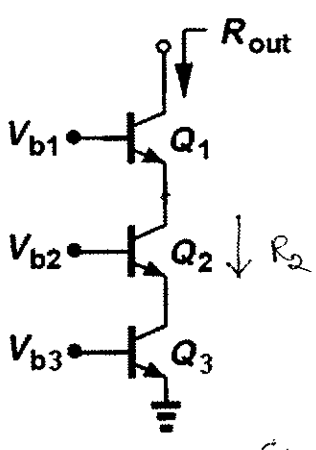
It can be used as a buffer stage between a CE stage and a small load.

Reason: Putting a CE stage directly to a small load degrades the gain. This particular stage gives high input impedance and low output resistance; thereby matching the impedance between CE stage and a small load.

b) [2 pts] How do cascodes help in amplifier design?

Cascodes boost the output impedance thereby increasing the gain.

c) [4 pts] What is the ***maximum*** output impedance of the following cascade?



$$R_{out} = r_{o1} + (1 + g_{m1} r_{o1})\{r_{\pi 1} \| R_2\} \approx g_{m1} r_{o1} (r_{\pi 1} \| R_2)$$

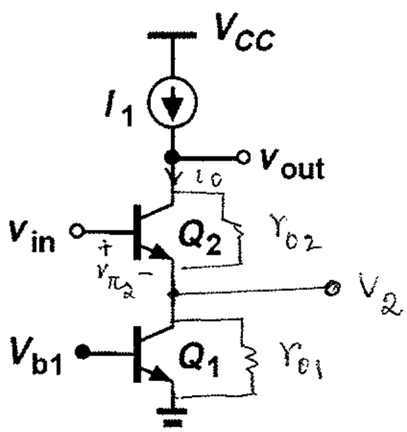
$$R_2 = r_{o2} + (1 + g_{m2} r_{o2})(r_{o3} \| r_{\pi 2})$$

$$\approx g_{m2} r_{o2} (r_{o3} \| r_{\pi 2})$$

Since, $R_2 \gg r_{\pi 2}$, $R_2 \| r_{\pi 1} \approx r_{\pi 1}$ $\therefore$ $R_{out} \approx g_{m1} r_{o1} r_{\pi 1}$

$R_{out,max} = \beta r_{o1}$

d) [4 pt] Explain why the following is not a good cascade. How will you change the design to obtain a larger small signal gain?



$$i_o = g_{m_2} v_{\pi_2}$$

$$= g_{m_2}(V_{in} - V_2)$$

$$V_2 = i_o\{r_{o1} \| r_{o2}\}$$

$$\therefore i_o = g_{m_2}\{V_{in} - i_o(r_{o1} \| r_{o2})\}$$

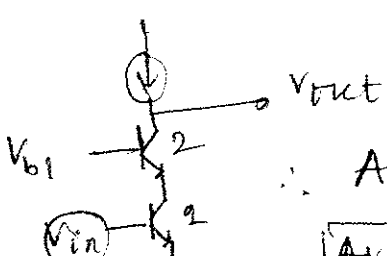
$$\Rightarrow \{1 + g_{m_2}(r_{o1} \| r_{o2})\} i_o = g_{m_2} V_{in}$$

$$\therefore G_m = \text{overall gain} = \frac{i_o}{V_{in}}$$

$$\boxed{G_m = \frac{g_{m_2}}{1 + g_{m_2}(r_{o1} \| r_{o2})}}$$

Hence overall gain is very small.

An easy way to solve this problem is to interchange V_{b1} and V_{in}

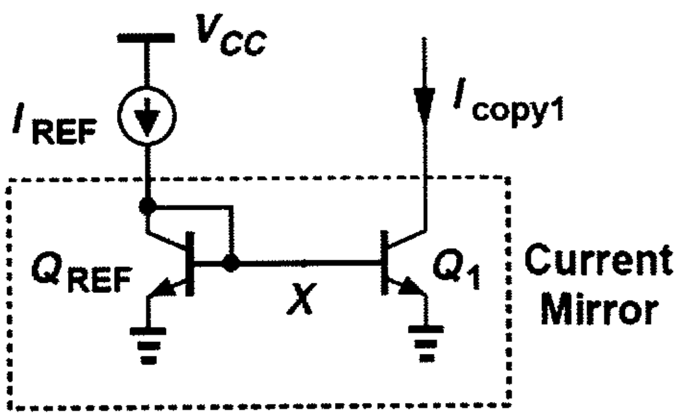


$$\therefore A_V = -g_{m_1}\{r_{o2} + (1 + g_{m_2} r_{o2})(r_{o1} \| r_{\pi_1})\}$$

$$A_V \approx -g_{m_1} g_{m_2} r_{o2} (r_{o1} \| r_{\pi_1})$$

PROB 3. Current mirrors and Frequency Response. [18 pts]

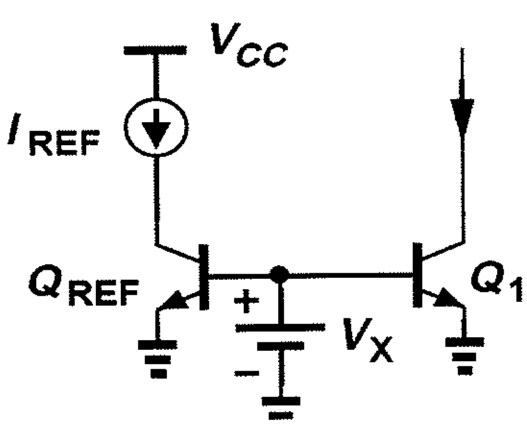
a) [3 pts] Neglecting base currents find I_{copy1} as a function of I_{Ref}



$$V_X = V_T \ln\left(\frac{I_{COPY1}}{I_{S_1}}\right) = V_T \ln\left(\frac{I_{REF}}{I_{S_{REF}}}\right)$$

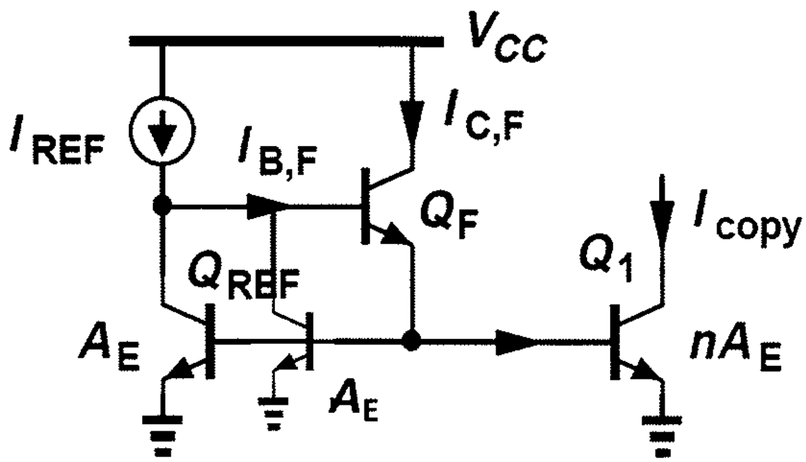
$$\therefore \boxed{I_{copy_1} = \frac{I_{S,1}}{I_{S_{REF}}} I_{REF}}$$

b) [3 pts] Why is the following not a good mirror?



Since V_X is fixed, ~~I_{REF}~~ a change in temp will affect I_{copy1}. Note that without the diode connection ~~Q~~ Q_{REF} and Q_1 are completely independ. V_C for Q_{REF} can be different than V_C at Q_1

c) [6 pts] For the following, derive an expression fo I_{copy} as a function of I_{Ref} ***including the base currents.***



$$I_{REF} = I_{BF} + 2I_{C_{REF}} \quad \text{— ①}$$

$$I_{C,F} \cong I_{EF} = \frac{2I_{copy}}{n\beta} + \frac{I_{copy}}{\beta}$$

$$I_{BF} = \frac{I_{copy}}{\beta^2}\left[\frac{2}{n} + 1\right] \quad \text{— ②}$$

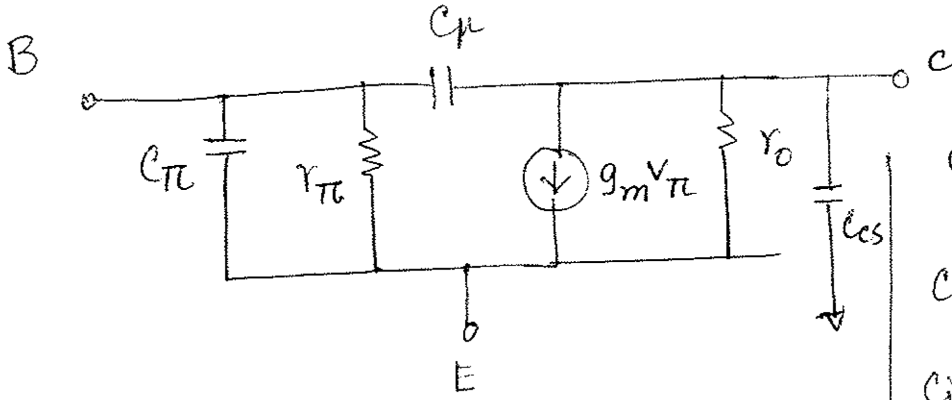
$$I_{C_{REF}} = \frac{I_{copy}}{n} \quad \text{— ③}$$

From ①, ② and ③

$$I_{REF} = I_{copy}\left[\frac{1}{\beta^2}\left\{\frac{2}{n} + 1\right\} + \frac{2}{n}\right]$$

$$\therefore \boxed{I_{copy} = \frac{n I_{REF}}{2 + \frac{1}{\beta^2}(n+2)}}$$

d) [2pts] Draw the high frequency model of a CE stage. Mention physical origins for each of the capacitances in this model.



$C_\pi = C_b + C_{je}$

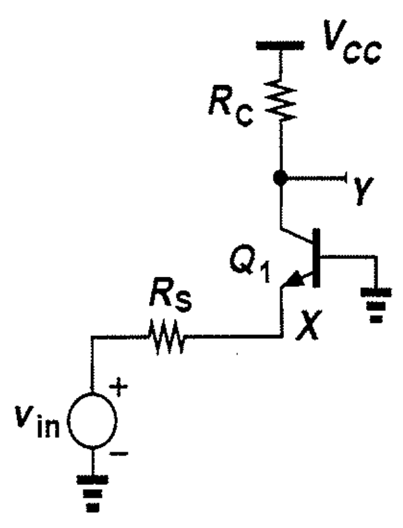
C_μ : depletion capacitance at collector junction

C_b : diffusion capacitance

C_{je} : depletion capacitance at emitter junction

C_{cs} : substrate capacitance

e) [4 pts] Find out the poles of the following circuit at nodes X and Y.



$$\omega_X \cong \frac{1}{\left(R_S \,||\, \frac{1}{g_m}\right) C_\pi}$$

$$\omega_Y \cong \frac{1}{R_C\,(C_\mu + C_{cs})}$$

Note that looking into Y:

$$R = R_C \,||\, \left(r_o + (1 + g_m r_o) R_S\right) \approx R_C$$