University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Final Examination

Spring 2000 Prof. Roger T. Howe May 13, 2000

_____,_____
Your Name (Last, First)

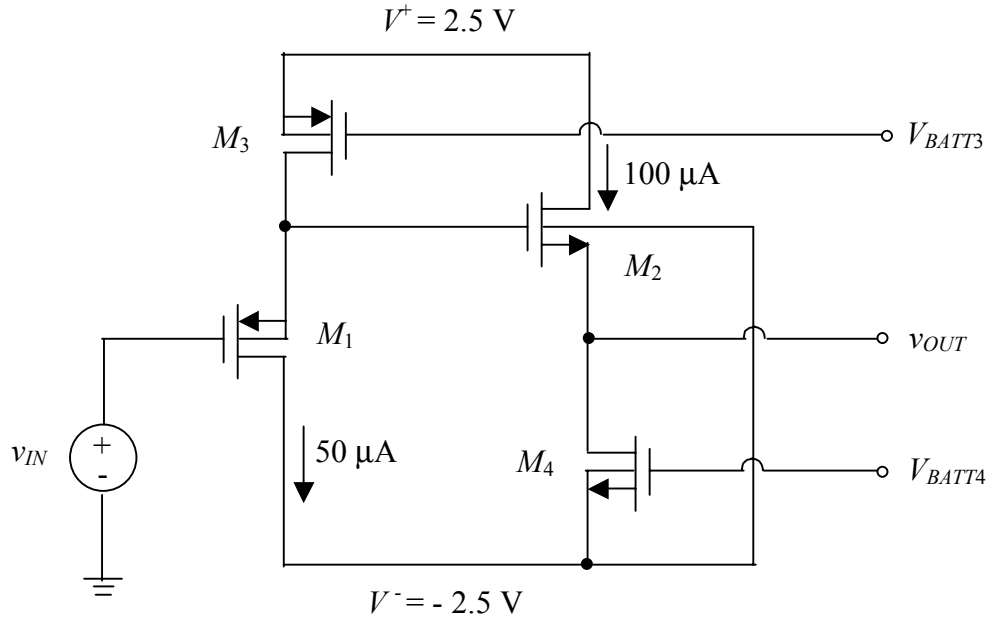
Guidelines

Closed book and notes; three 8.5" x 11" page (both sides) of *your own notes* is allowed.
You may use a calculator.
Do not unstaple the exam.
Show all your work and reasoning on the exam in order to receive full or partial credit.
You have 180 minutes (3 hrs.); use your time wisely. Good luck!

Score

Problem	Points Possible	Score
1	25	
2	25	
3	25	
4	25	
Total	100	

1. CMOS amplifier [25 points]



Given:

$\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{TOn} = 1.0$ V, $\gamma_n = 0.3\ V^{1/2}$, $2\phi_p = -1$ V, neglect λ_n

$\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{TOp} = -1.0$ V, $\gamma_p = 0.3\ V^{1/2}$, $2\phi_n = 1$ V, neglect λ_p

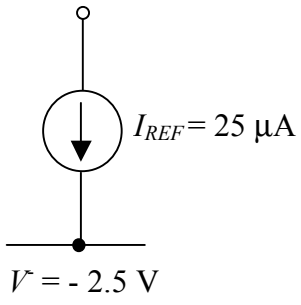
M_1: $(W/L)_1 = 32/2$ (μm/μm) M_4: $(W/L)_4 = 32/2$ (μm/μm)

M_3: $(W/L)_3 = 32/2$ (μm/μm)

(a) [4 pts.] What are the numerical values of the battery voltages V_{BATT3} and V_{BATT4} such that the drain currents of M_1 and M_2 are as shown on the schematic. The amplifier is biased such that all transistors are in MOSFET saturation.

(b) [4 pts.] We desire to have the DC output voltage $V_{OUT} = 0$ V when the DC input voltage $V_{IN} = 0$ V. What is the numerical value of the width of transistor M_2 needed to meet this specification, given that its channel length is $L = 2$ μm? Note that the backgate of transistor M_2 is *not* connected to its source.

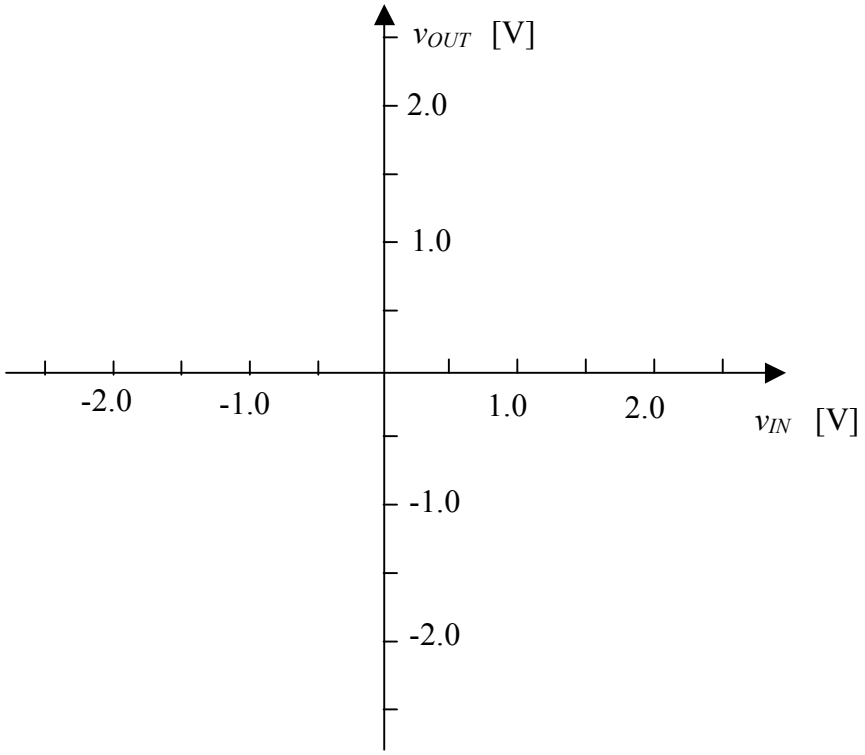
(c) [6 pts.] Design a circuit containing 3 MOSFETs that generates V_{BATT3} and V_{BATT4} from a single $I_{REF} = 25$ μA reference current "sink" to the negative supply voltage, as shown in the schematic below. Be sure to provide the (W/L) ratios for the three transistors, given that their channel lengths are all $L = 2$ μm.



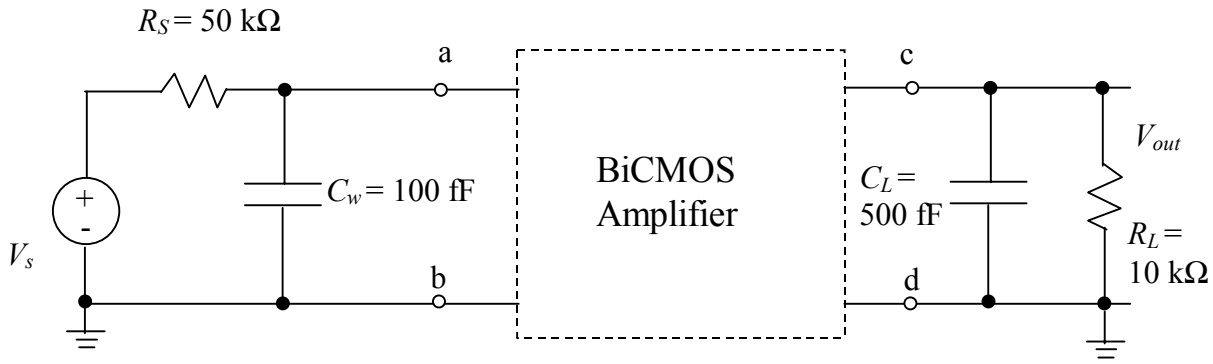
(d) [4 pts.] Find the numerical value of the maximum output voltage $V_{OUT(max)}$ in Volts, for which all transistors remain saturated. If you couldn't solve (a) and (b), assume for this part that $V_{BATT3} = 1.2$ V, $V_{BATT4} = -1.2$ V, and $(W/L)_2 = 50/2$ (μm/μm). Note that you do not need the answer to part (c) to do this part!

(e) [4 pts.] Find the numerical value of the minimum output voltage $V_{OUT(min)}$ in Volts, for which all transistors remain saturated. If you couldn't solve (a) and (b), assume for this part that $V_{BATT3} = 1.2$ V, $V_{BATT4} = -1.2$ V, and $(W/L)_2 = 50/2$ (μm/μm). Note that you do not need the answer to part (c) to do this part!

(f) [3 pts.] Sketch the transfer curve v_{OUT} versus v_{IN}. You need only consider the large-signal behavior of the circuit in determining the approximate slope at $v_{IN} = 0$; there is no need to do small-signal analysis.



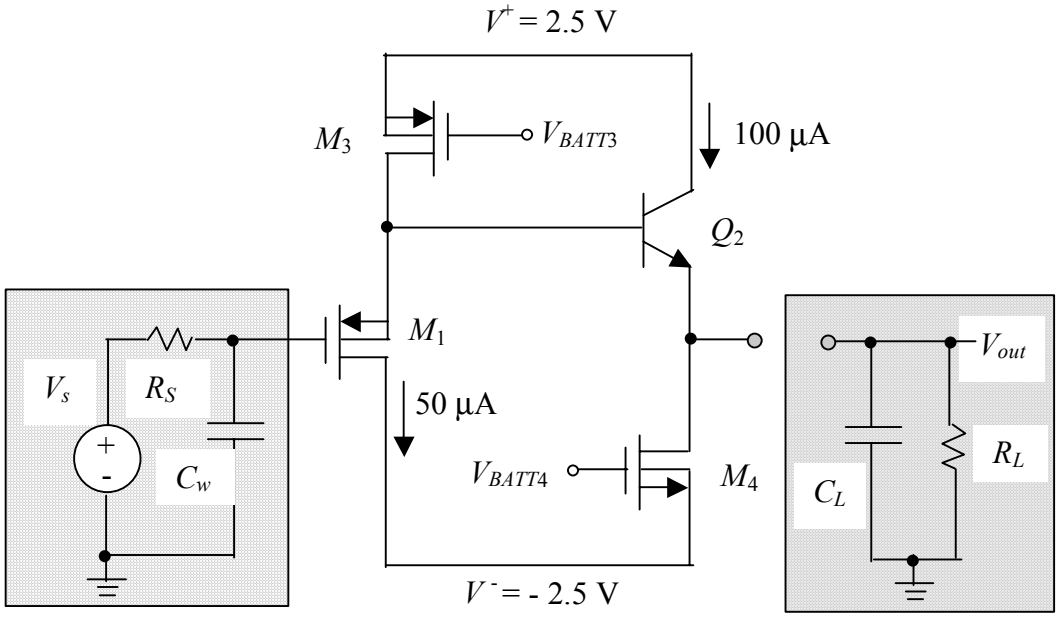
2. Frequency Response [25 points]



(a) [3 pts.] After a frustrating effort to bias the amplifier, you give up and directly connect terminal pair a-b to terminal pair c-d, eliminating the amplifier from the circuit. Find the transfer function V_{out} / V_{in} as a function of the radian frequency ω. Express the transfer function in the standard one-pole form; there is no need to substitute for the numerical values of the resistors and capacitors.

(b) [3 pts.] The source voltage is the cosine function $v_s(t) = 25mV \cos[2\pi(25MHz)t]$. Using your result from part (a), find the output voltage $v_{out}(t)$. If you couldn't solve part (a), you can assume that the transfer function is 0.5 at low frequency and that the –3 dB frequency is 50 MHz.

(c) [4 pts.] You decide to try the BiCMOS amplifier again and this time, you get it biased correctly. The load is a small-signal model of the actual load and is only connected for analyzing the small-signal gain of the amplifier.



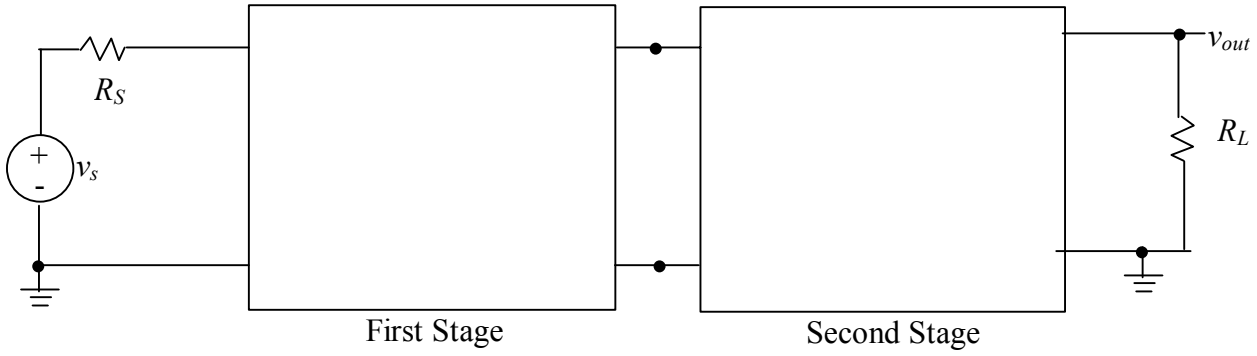
$\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{TOn} = 1.0$ V, $\gamma_n = 0.5\ V^{1/2}$, $2\phi_p = -1$ V, $\lambda_n = 0.05\ V^{-1}$
$C_{ox} = 2\ fF/\mu m^2$, $C_{ov} = 0.4$ fF/μm of gate width

$\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{TOp} = -1.0$ V, $\gamma_p = 0.5\ V^{1/2}$, $2\phi_n = 1$ V, $\lambda_p = 0.05\ V^{-1}$
$C_{ox} = 2\ fF/\mu m^2$, $C_{ov} = 0.4$ fF/μm of gate width

$(W/L)_1 = (W/L)_3 = (W/L)_4 = 32/2$ (μm/μm)

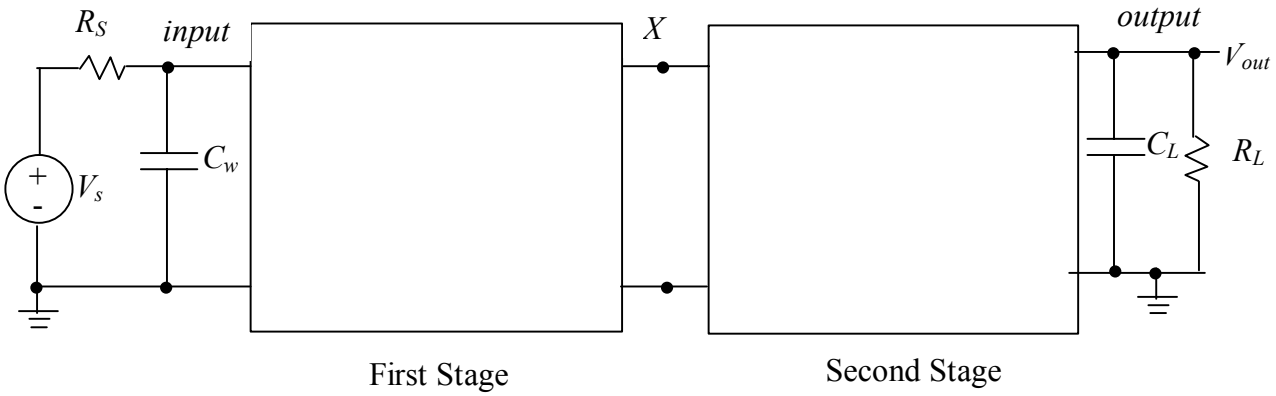
$\beta_o = 100$, $V_{An} = 50$ V, $C_{jE} = 25$ fF, $\tau_F = 45$ ps, $C_\mu = 25$ fF

Draw the low-frequency (no capacitors) two-port cascaded model for this two-stage amplifier below. Substitute for the two-port parameters (e.g., R_{out1} of stage 1) in terms of the small-signal device parameters (e.g., r_{o1}, r_{o3}, etc.). Write neatly!



(d) [3 pts.] Find the numerical value of the overall, loaded low frequency voltage gain of this amplifier v_{out}/v_s with R_S = 50 kΩ and R_L = 10 kΩ. Answers that are accurate to within 5% will receive full credit.

(e) [3 pts.] Add the intrinsic device capacitances C_{gs}, C_{gd}, C_π, and C_μ for the MOSFETs and the bipolar transistor onto the appropriate nodes of the two-port model of the two-stage amplifier. Do *not* add the parasitic device capacitances C_{db} and C_{cs}. Write neatly!

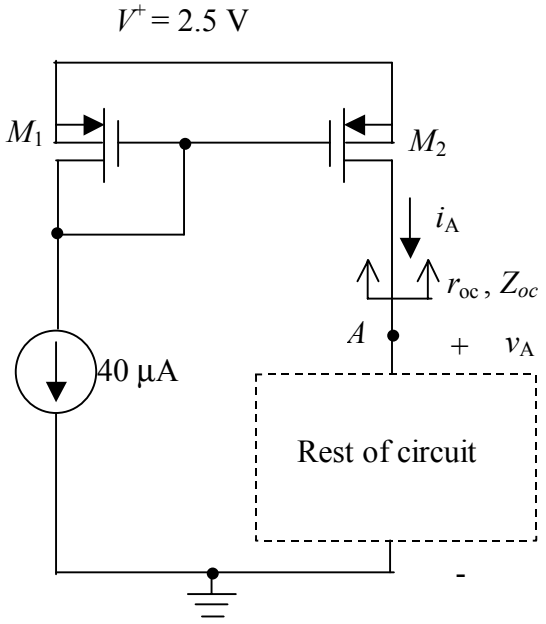


(f) [3 pts.] What is the numerical value of the open-circuit time constant for the capacitance from the input node to ground? Your result should include the contribution of any Miller capacitors that are present at the input node. Answers that are accurate to within 5% will receive full credit.

(g) [3 pts.] What is the numerical value of the open-circuit time constant for the capacitance from node X to ground? Your result should include the contribution of any Miller capacitors that are present at node X. Answers that are accurate to within 5% will receive full credit.

(h) [3 pts.] What is the numerical value of the –3 dB frequency (in Hertz) of this amplifier, according to the open-circuit time constant method? If you couldn't solve parts (f) and (g), you can assume that the time constant for the input node is 1.2 ns and that for node *X* is 0.7 ns. Answers that are accurate to within 5% will receive full credit.

3. Current supplies [25 points]



$\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{TOp} = -1.0$ V, $\lambda_p = 0.1 / L\ V^{-1}$
$C_{ox} = 2\ fF/\mu m^2$, $C_{ov} = 0.4$ fF/µm of gate width
$C_{jo} = 0.2\ fF/\mu m^2$, $\phi_{Bp} = 1$ V, $C_{jswo} = 0$.
$L_{diff} = 6$ µm

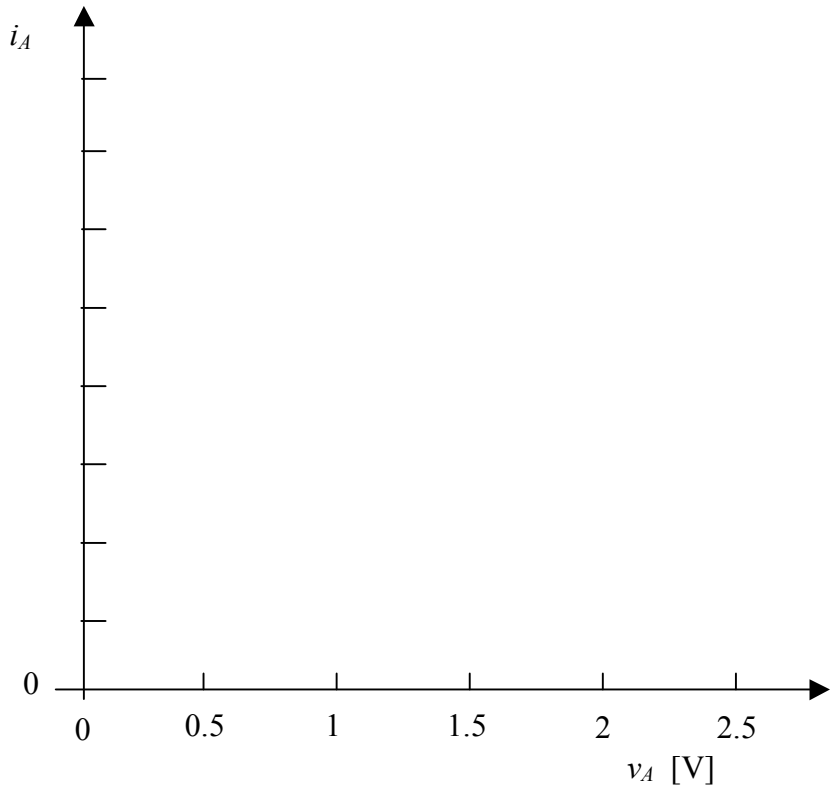
$(W/L)_1 = 8\ \mu m / 2\ \mu m$

$(W/L)_2 = 8$ W_2 and L_2 to be determined

(a) [3 pts.] Find the numerical value of $I_A = -I_{D2}$ when both MOSFETs are in their constant-current (saturation) regions.

(b) [3 pts.] Find the minimum integer value of the channel length L_2 of transistor M_2 (in µm), such that the small-signal resistance r_{oc} of the current supply is *at least* 500 kΩ.

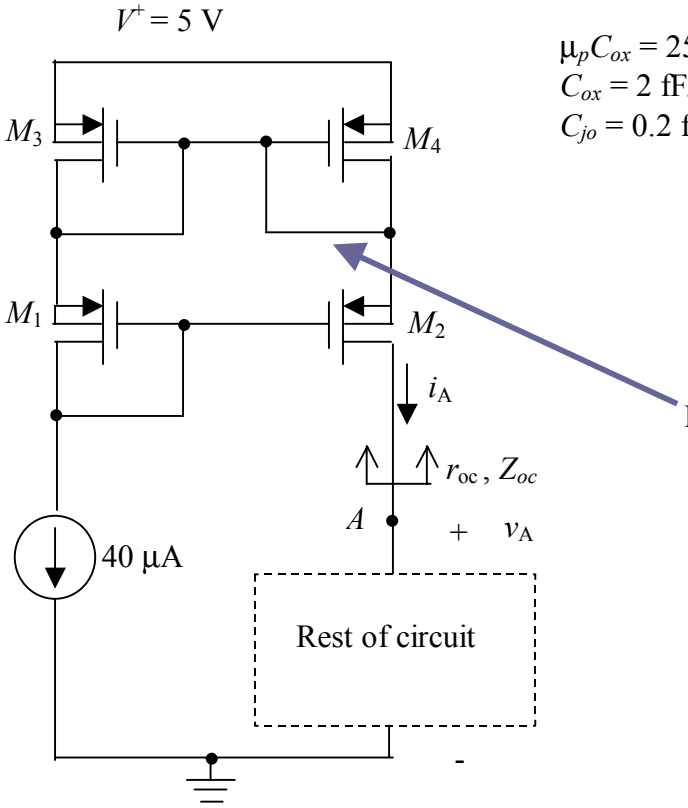
(c) [3 pts.]Plot the current i_A versus the voltage v_A over the range 0 V to 2.5 V on the graph below. You do not need to account for channel-length modulation.



(d) [4 pts.] What is the numerical value of the capacitance C_a from node A to ground in fF? You should include any capacitors from node A to "battery-like" nodes. *Given*: the DC voltage at A is $V_A = 1.25$ V. If you couldn't solve part (b), you can assume that the width of M_2 is $W_2 = 40$ μm.

(e) [4 pts.] At what frequency (in Hz) is the magnitude of the impedance Z_{oc} equal to 300 kΩ? If you couldn't solve parts (b) and (d), you can assume that r_{oc} = 525 kΩ and that C_a = 100 fF.

(f) [4 pts.] Consider the "improved" current supply below. Due to a layout error, the gate and drain of M_4 are connected. What is the maximum voltage $V_{A(max)}$ for which M_2 remains in the constant-current (saturation) region?



$\mu_p C_{ox}$ = 25 µA/V^2, V_{TOp} = -1.0 V, λ_p = 0.1 / L V^{-1}
C_{ox} = 2 fF/µm^2, C_{ov} = 0.4 fF/µm of gate width
C_{jo} = 0.2 fF/µm^2, ϕ_{Bp} = 1 V, C_{jswo} = 0.

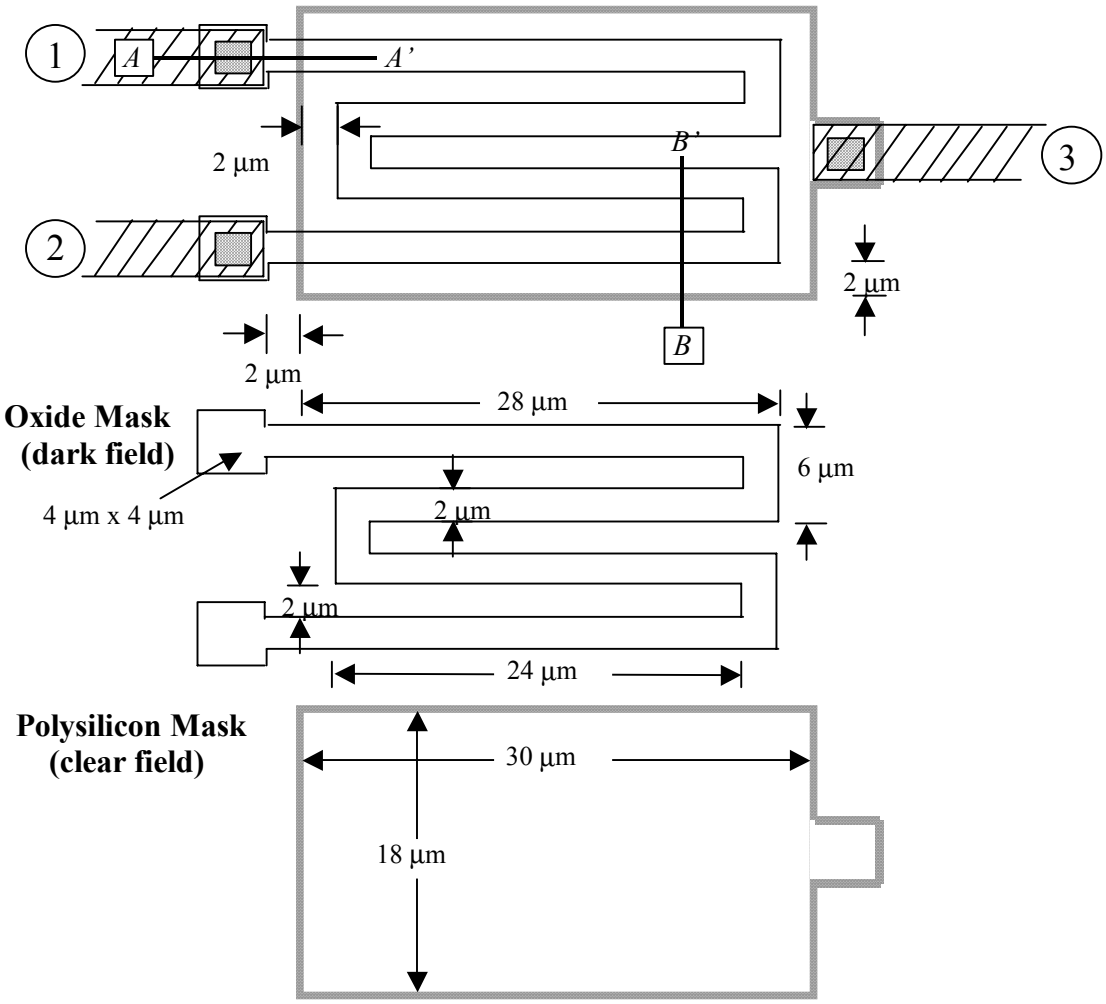
$(W/L)_1 = (W/L)_3$ =8 µm / 2 µm

$(W/L)_2 = (W/L)_4$ =16 µm / 2 µm

Layout error

(g) [4 pts.] What is the numerical value of the small-signal resistance r_{oc} for the "improved" current supply?

4. MOSFET device structure [25 points]

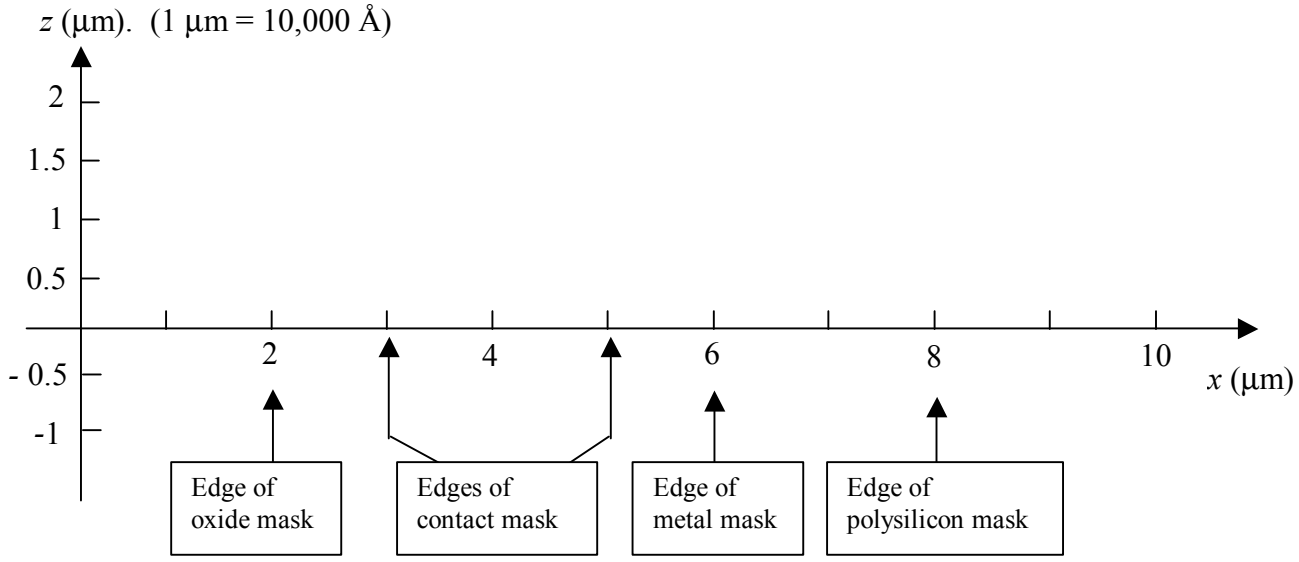


Contact and Metal Masks:
(contact: dark field); (metal: clear field)

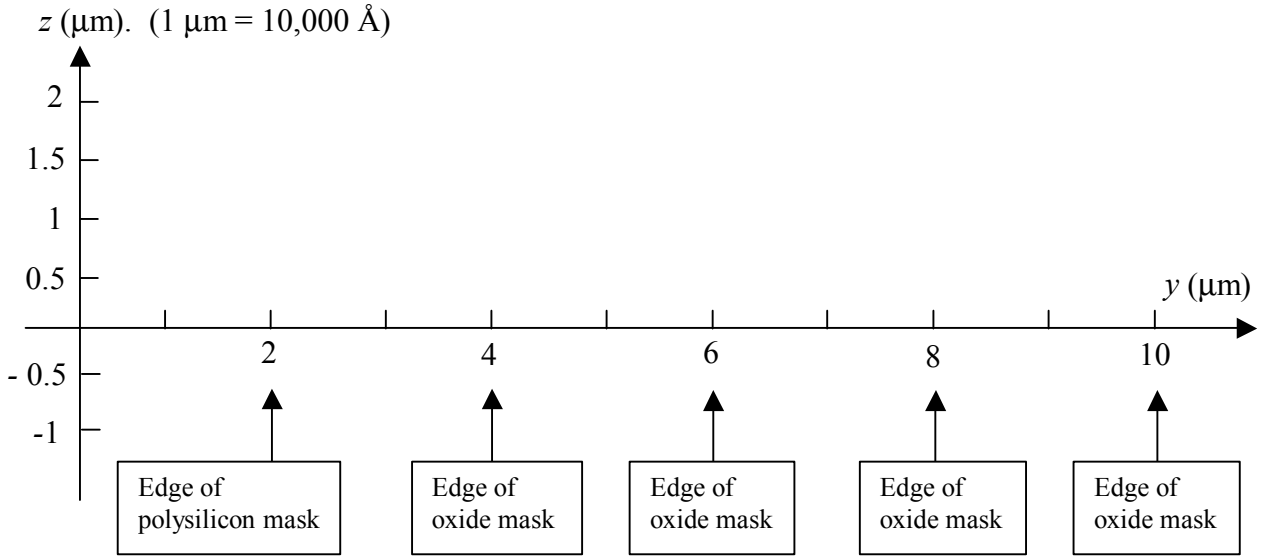
Process Recipe

1. Starting material: p-type silicon wafer with doping concentration $N_a = 10^{17}$ cm^{-3}.
2. Grow 5000 Å of thermal SiO_2 and pattern with the **oxide mask** (dark field).
3. Grow 150 Å of thermal SiO_2.
4. Deposit 3000 Å of n+ polysilicon and pattern with the **polysilicon mask** (clear field).
5. Ion implantation: phosphorus, dose $Q_d = 10^{14}$ cm^{-2}. Anneal to form doped regions with junction depth of 5000 Å.
6. Deposit 5000 Å of CVD SiO_2 and pattern with the **contact mask** (dark field).
7. Deposit 5000 Å of aluminum and and pattern with the **metal mask** (clear field).

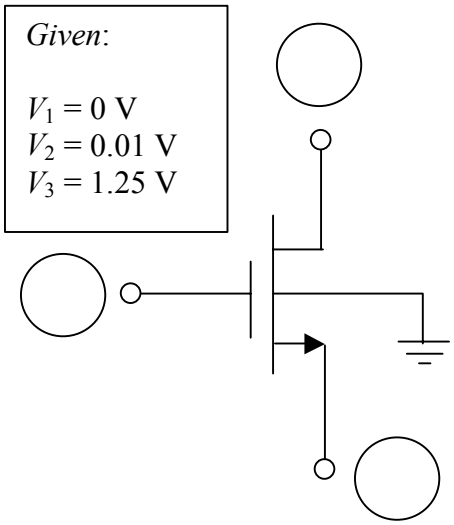
(a) [5 pts.] Draw the cross section $A - A'$ on the axes below. Label all the layers and *find the carrier type and concentration of the implanted regions*. The locations of the mask edges have been indicated on the x axis scale for your convenience.



(b) [5 pts.] Draw the cross section $B - B'$ on the axes below. Label all the layers. The locations of the mask edges have been indicated on the y axis scale for your convenience.



(c) [5 pts.] (i) Fill in the circles with the terminal numbers from the layout , (ii) circle the operating region of the MOSFET for the given terminal voltages, and (iii) give the width and length of the channel in μm.. The substrate (backgate) is grounded.



Operating Region (circle one)

Triode Saturation

Channel width (μm):

Channel length (μm):

(d) [5 pts.] The mobility of the electrons in the channel is measured to be $\mu_n = 325\ cm^2/(Vs)$, the permittivity of oxide is $\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm, and the threshold voltage is $V_{Tn} = 1$ V. What is the numerical value of the drain current I_D for the bias voltages given in part (c)?

(e) [5 pts.] What is the numerical value of the capacitance between node 3 and ground, for the bias conditions given in part (c)? You can neglect the capacitance between the aluminum metal line, but you should include *all* capacitance between the polysilicon layer and ground. Given: the permittivity of silicon is $\varepsilon_s = 1.035 \times 10^{-12}$ F/cm and the depletion region under the 5000 Å-thick oxide at the given bias voltages is 200 Å thick.