University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Final Examination

Spring 2002 Prof. Roger T. Howe May 18, 2002

_____,_____
Your Name (Last, First)

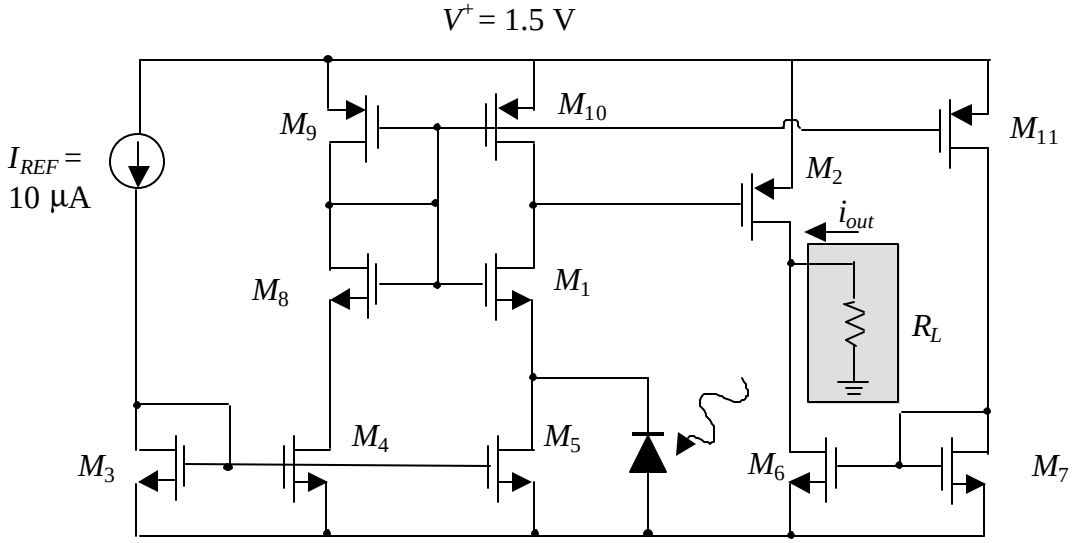
Guidelines

Closed book and notes; three 8.5" x 11" page (both sides) of *your own notes* is allowed.
You may use a calculator.
Do not unstaple the exam.
Show all your work and reasoning on the exam in order to receive full or partial credit.
You have 180 minutes (3 hrs.); use your time wisely. Good luck!

Score

Problem	Points Possible	Score
1	30	
2	25	
3	25	
4	20	
Total	100	

1. CMOS two-stage photocurrent amplifier [30 points]



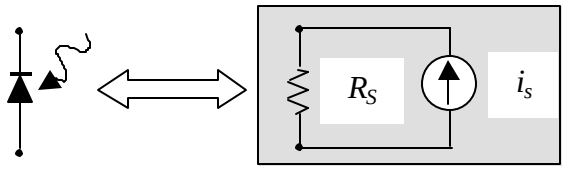
Given:

$\mu_n C_{ox} = 50\ \mu A/V^2$, $V_{Tn} = 1.0$ V, $\lambda_n = 0.05\ V^{-1}$

$\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{Tp} = -1.0$ V, $\lambda_p = 0.05\ V^{-1}$

Neglect the backgate effect.

Illuminated Photodiode Model:



$R_S = 100\ k\Omega$
$R_L = 100\ k\Omega$

M_1: $(W/L)_1 = 256/1$ (μm/μm)

M_2: $(W/L)_2 = 256/1$ (μm/μm)

M_3: $(W/L)_3 = 16/1$ (μm/μm)

M_4: $(W/L)_4 = 32/1$ (μm/μm)

M_5: $(W/L)_5 = 256/1$ (μm/μm)

M_6: $(W/L)_6 = 128/1$ (μm/μm)

M_7: $(W/L)_7 = 32/1$ (μm/μm)

M_8: $(W/L)_8 = 32/1$ (μm/μm)

M_9: $(W/L)_9 = 64/1$ (μm/μm)

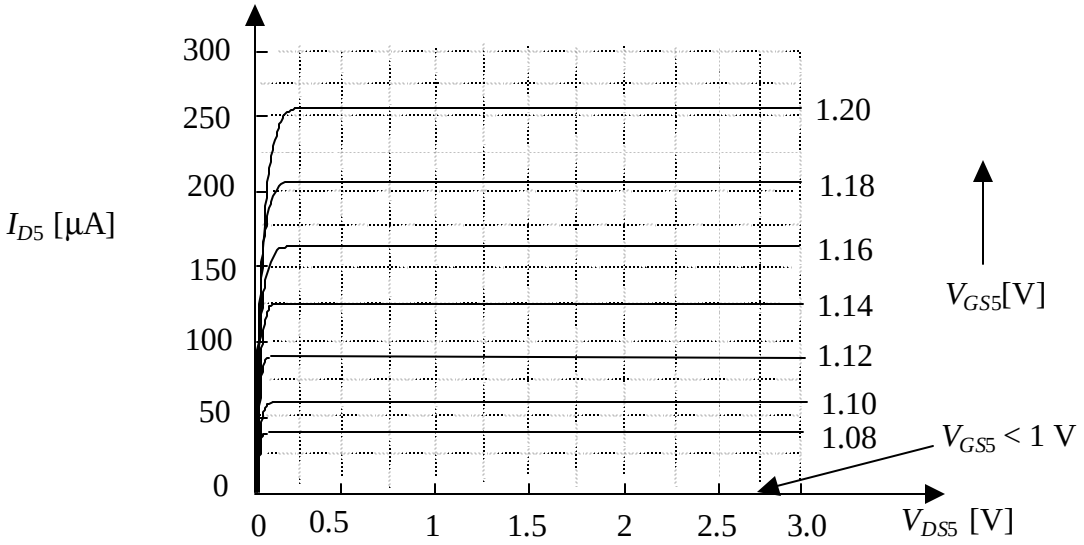
M_{10}: $(W/L)_9 = 512/1$ (μm/μm)

M_{11}: $(W/L)_9 = 64/1$ (μm/μm)

(a) [3 pts.] Find the numerical values of the DC drain currents for transistors M_1, M_{10}, and M_2. You can assume that all transistors are saturated, that the DC output voltage is $V_{OUT} = 0$ V, and that channel length modulation can be neglected.

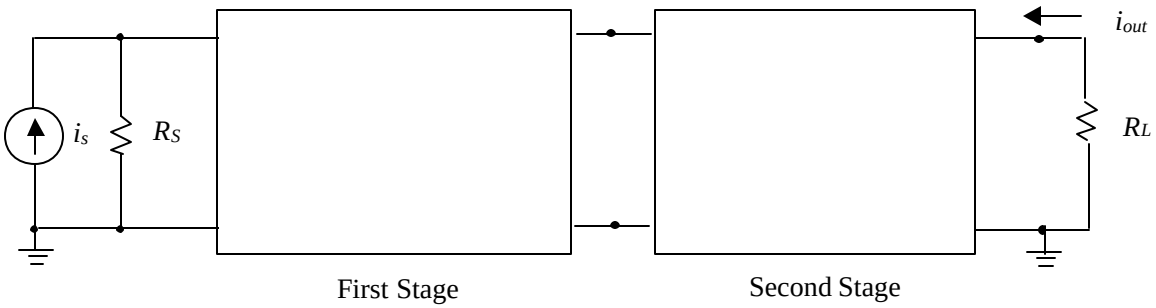
I_{D1} = _____ μA	$-I_{D10}$ = _____ μA	$-I_{D2}$ = _____ μA

(b) [3 pts.] Locate the bias point Q, which is the point $I_{D5}(V_{GS5}, V_{DS5})$, for transistor M_5 on the family of curves on the plot below. Select the nearest V_{GS5} curve from those given on the plot.



(c) [5 pts.] Redraw the circuit with non-ideal ("gray circle") current supplies and any bias current sources or voltage sources for each amplifier stage. Label with the numerical values of the DC currents I_{SUP} and I_{BIAS} and the DC voltage V_{DC}. There is no need to evaluate the resistances r_{oc}. *Hint*: your circuit should contain two current supplies, one bias current, and one bias voltage.

(d) [4 pts.] Identify the two-port type for each amplifier stage (e.g., CS, CG, or CD) and fill in the appropriate circuit model (e.g., current buffer, transconductance amp, etc.). You should include the elements (e.g., R_{in}, R_{out}, gain element) for each stage in your circuit. There is no need to evaluate any of the parameters for this part.



(e) [3 pts.] Find the numerical value of the input resistance R_{in} of this amplifier in Ohms. You should make reasonable approximations to simplify the calculations.

R_{in} = _____Ω

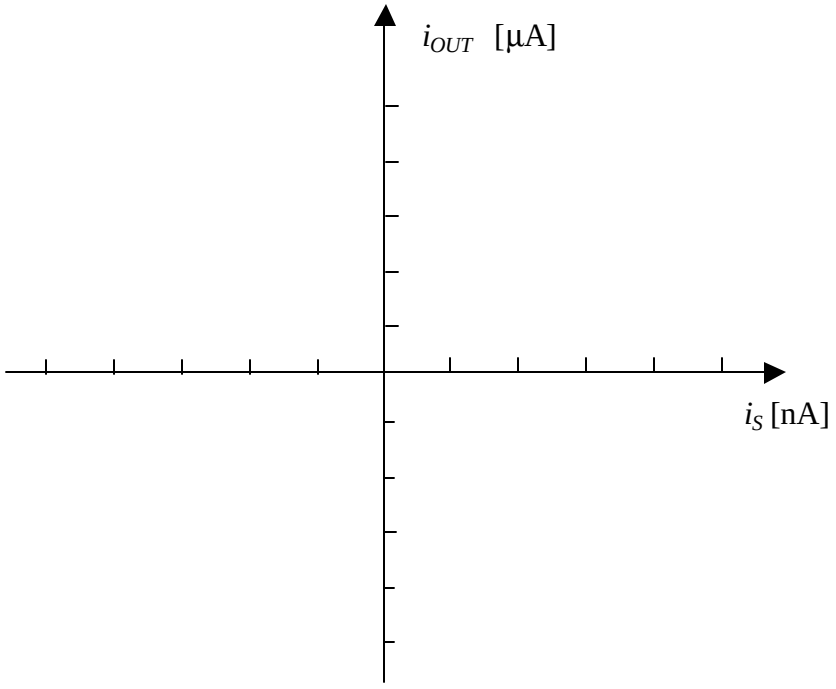
(f) [5 pts.] Find the numerical value of A_i (the low-frequency short-circuit current gain -- a two-port parameter.) Again, you should make reasonable approximations in order to save time and pencil lead!

A_i = _____

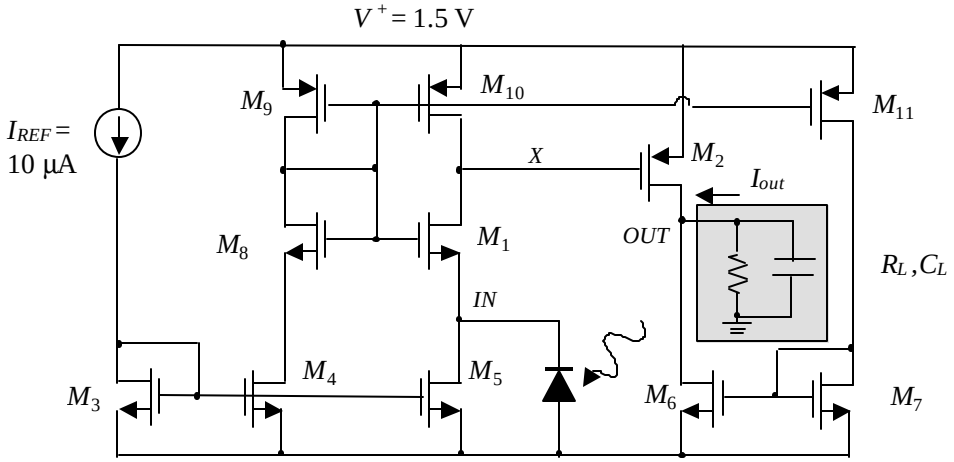
(g) [4 pts.] Find the maximum *amplitude* $\hat{i}_{OUT,MAX}$ of the output current $i_{OUT,}(t)$ in μA which avoids clipping. Note that the value of the load resistor is R_L = 100 kΩ.

$\hat{i}_{OUT,MAX}$ = _____ μA

(h) [3 pts.] Sketch the transfer curve $\boldsymbol{i_{OUT}}$ **vs.** $\boldsymbol{i_S}$ where the output current is in μA and the input current is in nA = 10^{-9} A. Consider the input source to be "large signal" for this part and neglect R_S. Provide your own appropriate scale -- your sketch should be consistent with your answers to parts (f) and (g). If you couldn't solve these parts, you can assume that the overall short-circuit current gain is 75 and that -1.2 V < v_{OUT} < 0.9 V (not the correct answers, of course).



2. Frequency Response of a CMOS Photocurrent Amplifier [25 points]



Given:

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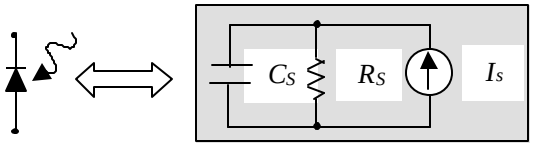
$\mu_p C_{ox} = 25\ \mu A/V^2$, $V_{Tp} = -1.0$ V, $\lambda_p = 0.05\ V^{-1}$

Illuminated Photodiode Model:



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M_8: $(W/L)_8 = 32/1$ (μm/μm)

M_9: $(W/L)_9 = 64/1$ (μm/μm)

M_{10}: $(W/L)_9 = 512/1$ (μm/μm)

$R_S = 100$ kΩ
$C_S = 100$ fF
$R_L = 100$ kΩ
$C_L = 100$ fF

Device Capacitance Data: $C_{ox} = 2$ fF/μm^2, $C_{ov} = 0.1$ fF/μm, $L_{diff} = 2$ μm,
NMOS: $C_{db} = 0.5$ fF/μm^2, PMOS: $C_{db} = 0.3$ fF/μm^2

(a) [4 pts.] What is the numerical value of the total capacitance C_{in} between the input node *IN* and small-signal ground (in fF)? You can consider any node connected to a DC voltage source through a diode-connected MOSFET to be effectively at small-signal ground. Also, assume $V_{SB1} = 0$ V. List all relevant capacitances symbolically (e.g., C_{gs1}) before calculating their values.

C_{in} = _____fF

(b) [3 pts.] What is the open-circuit time-constant τ_{in} associated with C_{in} (in nanoseconds, 10^{-9} s)? If you couldn't solve problem 1(e), you can assume that the input resistance R_{in} = 2.5 kΩ for this part.

τ_{in} = _____ns

(c) [5 pts.] By using Miller's theorem and including all relevant capacitors, what is the total capacitance C_X between node X and small-signal ground (in fF)? You can consider any node connected to a DC voltage source through a diode-connected MOSFET to be effectively at small-signal ground. List all relevant capacitances symbolically (e.g., C_{gd1}) before calculating their values.

C_X = _____fF

(d) [2 pts.] What is the open-circuit time-constant τ_X associated with C_X (in nanoseconds, 10^{-9} s)? If you couldn't solve problem 1(f), you can assume that the short-circuit current gain $A_i = 105$.

τ_X = _____ns

(e) [3 pts.] What is the numerical value of the total capacitance C_{out} between the output node *OUT* and small-signal ground (in fF)? You can consider any node connected to a DC voltage source through a diode-connected MOSFET to be effectively at small-signal ground. List all relevant capacitances symbolically (e.g., C_{gd6}) before calculating their values.

C_{out} = _____fF

(f) [3 pts.] What is the numerical value of the open-circuit time constant τ_{out} for the capacitance between the output node *OUT* and small-signal ground (in nano-seconds, 10^{-9} s)?

τ_{out} = _____ns

(g) [3 pts.] What is the –3dB frequency ω_1 for this amplifier in Mrad/s, according to the open-circuit time constant method? If you couldn't do parts (a)-(f), you can assume here that C_{in} = 120 fF, C_X = 225 fF, and τ_{out} = 35 ns – all incorrect answers, of course.

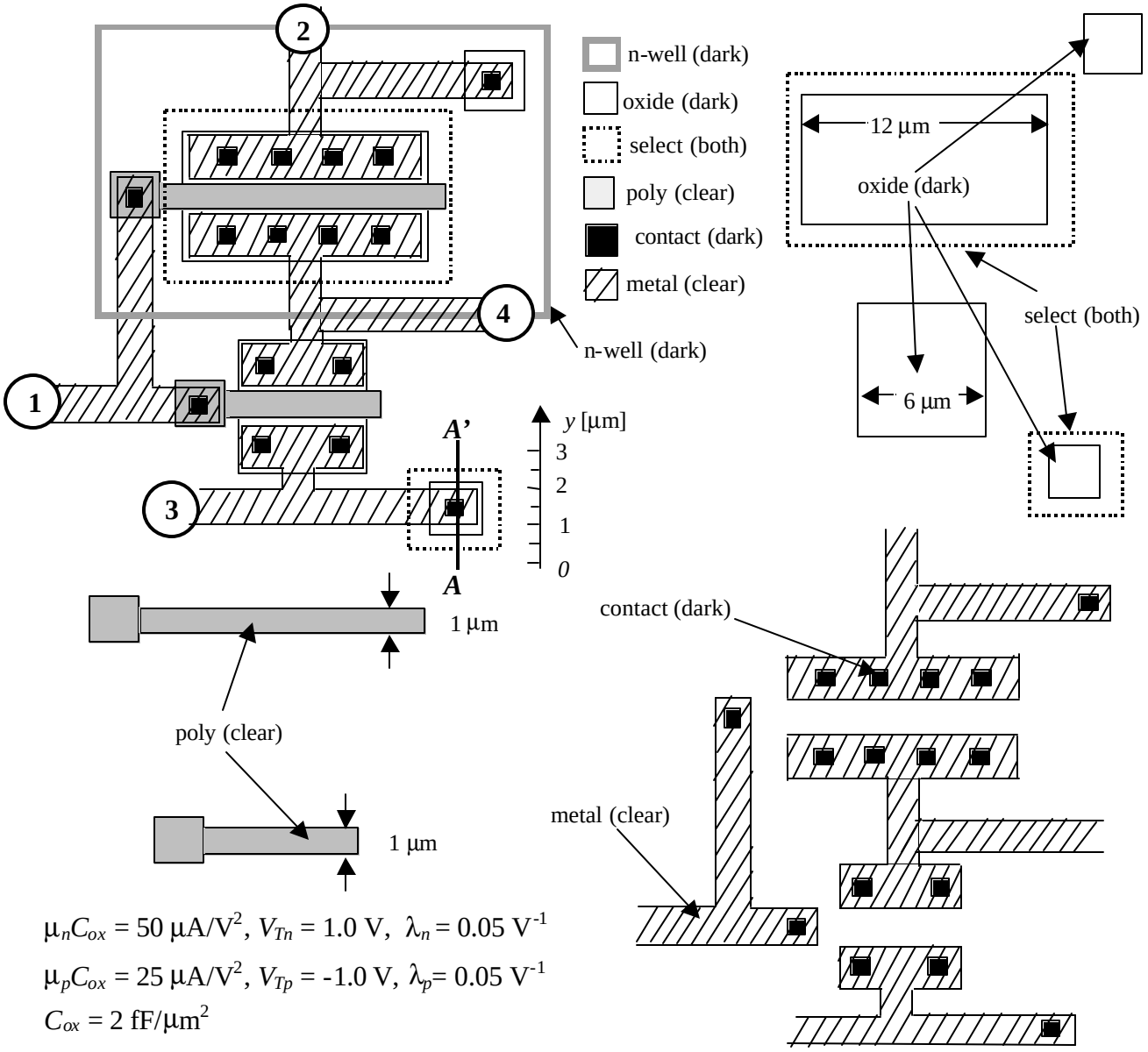
ω_1 = _____Mrad/s

(h) [2 pts.] The bandwidth is not high enough, so you decide to add a 3rd stage. Which CMOS 3rd stage, if any, would improve the bandwidth of this amplifier? Circle one answer and justify it.

Circle one: 1. CS 2. CG 3. CD 4. None

Justify your choice in one or two sentences:

3. New CMOS amplifier configuration [25 points]



$\mu_n C_{ox}$ = 50 µA/V^2, V_{Tn} = 1.0 V, λ_n = 0.05 V^{-1}

$\mu_p C_{ox}$ = 25 µA/V^2, V_{Tp} = -1.0 V, λ_p= 0.05 V^{-1}

C_{ox} = 2 fF/µm^2

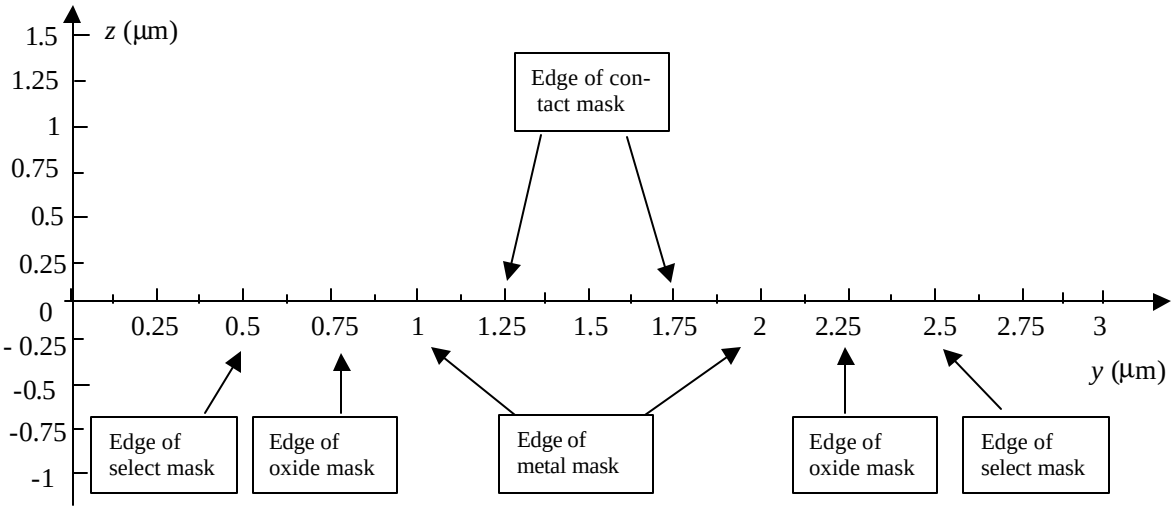
Node Voltages:
1: Input, 2: V_{DD} = 2.5 V, 3: V_{SS} = 0 V; 4: Output

n-well CMOS process: starting material: boron-doped silicon, conc. 1 x 10^{16} cm^{-3}

1. Deposit 500 nm of thermal silicon dioxide and pattern using the **well mask**
2. High-energy phosphorus implant; rapid-thermal anneal to form 2 µm-deep well with only a 0.5 µm-wide lateral spread of phosphorus under the well mask pattern (through the end of the process)
3. Etch off oxide, deposit 500 nm of silicon dioxide, pattern with **oxide mask**
4. Grow a 2.5 nm-thick gate oxide

5. Deposit 250 nm of heavily phosphorus-doped polysilicon and pattern with **poly mask**
6. Implant boron using photoresist patterned with the **select mask (dark field)** as an implant mask; strip resist.
7. Implant arsenic using photoresist patterned with the **select mask (clear field)** as an implant mask; strip resist.
8. Rapid-thermal anneal to form 0.25 µm-deep regions that spread laterally by L_D = 0.1 µm. Net doping conc. for both n and p type source/drain regions: 5 x 10^{18} cm^{-3}. The polysilicon layer is n-type at the end of this step.
9. Deposit 500 nm of silicon dioxide and etch 502.5 nm of oxide with the **contact mask**
10. Deposit 500 nm of aluminum and pattern using the **metal mask** (clear field).

(a) [5 pts.] Draw the cross section along ***A-A'*** on the graph below. The locations of the mask edges have been indicated on the *x* axis scale for your convenience. Label any ion-implanted regions in the substrate.



(b) [4 pts.] Draw the schematic of the circuit corresponding to this layout, including the connections for all four terminals and the (*W*/*L*) ratios of any MOSFETs in the circuit. Note that nodes 1-4 are defined below the schematic on p. 11.

(c) [4 pts.] Find the numerical value of the DC bias voltage V_{BIAS} between nodes 1 and 3 that is needed for the DC output voltage (node 4) to equal $V_{DD}/2 = 2.5/2$ V = 1.25 V. MOSFET parameters are listed below the schematic on p. 11. You can neglect channel-length modulation for this part.

V_{BIAS} = _____ V

(d) [4 pts.] Find the numerical value of the short-circuit transconductance G_m for this amplifier, when biased at the operating point specified in part (c). If you couldn't solve part (c), you can assume that any MOSFETs in the circuit are biased at a drain current $|I_D| = 20$ μA.

G_m = _____ μS

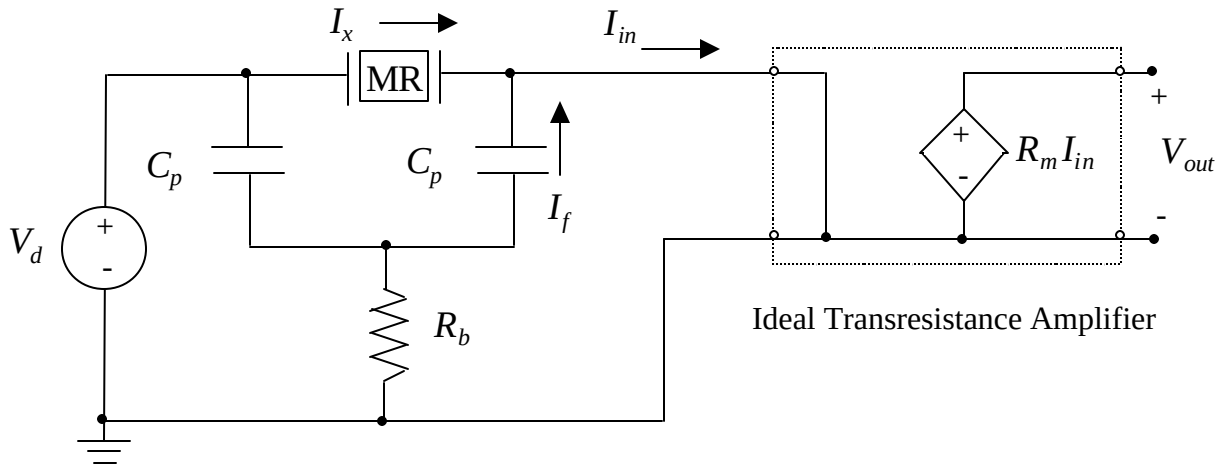
(e) [4 pts.] Find the numerical value of the output resistance of this amplifier, when biased at the operating point specified in part (c). If you couldn't solve part (c), you can assume that any MOSFETs in the circuit are biased at a drain current $|I_D| = 20\ \mu A$.

R_{out} = _____kΩ

(f) [4 pts.] What is the input capacitance C_{in} of this amplifier in fF when biased at the operating point specified in part (c), for the case where R_L is infinity? The input capacitance is the total capacitance (including any Miller capacitance) between the input (node 1) and small-signal ground.) If you couldn't solve part (c), you can assume that any MOSFETs in the circuit are biased at a drain current $|I_D| = 20\ \mu A$.

C_{in} = _____fF

4. Feedthrough model [20 points]



This circuit model represents substrate feedthrough around a MEMS resonator (MR).

(a) [5 pts.] Find an expression for the phasor feedthrough current I_f in terms of the drive voltage V_d. Do *not* simplify the expression for this part.

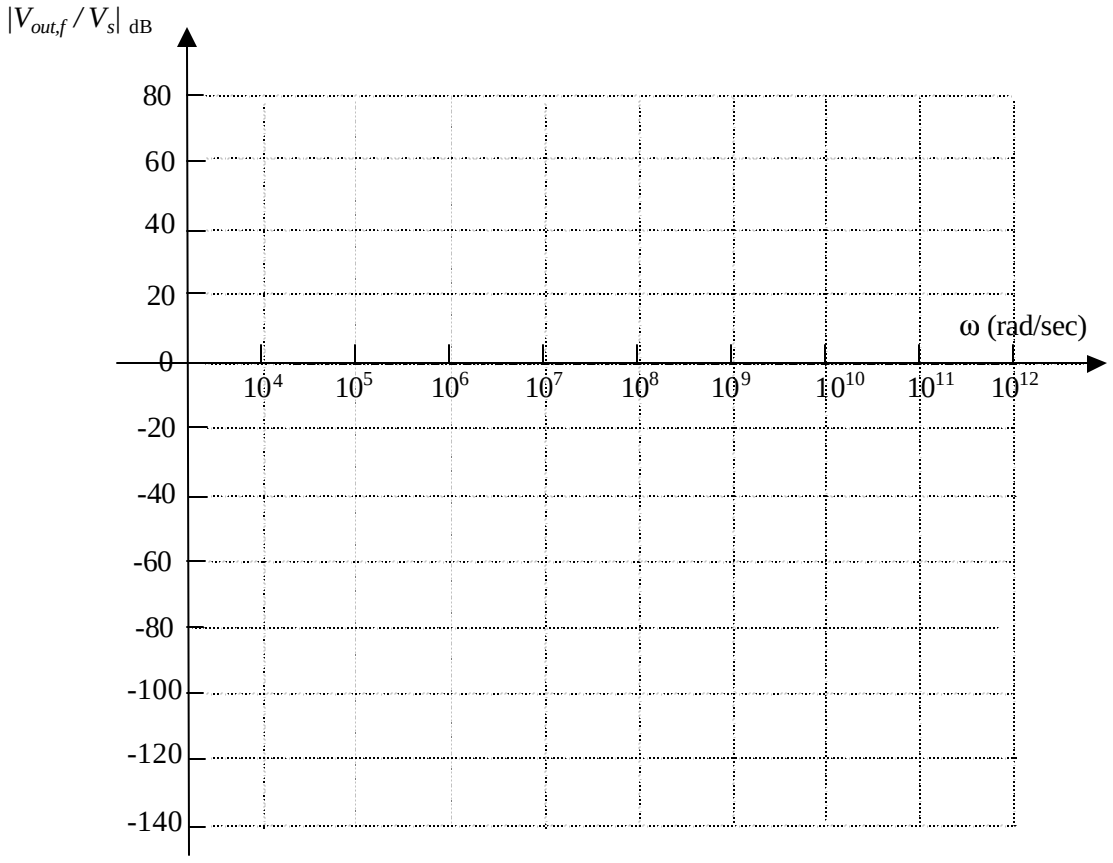
(b) [5 pts.] Find an expression for the output voltage $V_{out,f}$ due to I_f (that is, with I_x set to 0 A). Your answer should be expressed as $V_{out,f} / V_d$ and must be reduced to the form of one pole and a numerator proportional to ω^2.

(c) [5 pts.] On the graph below, plot the magnitude Bode Plot for the transfer function $V_{out,f} / V_d$. The parameters are: C_p = 500 fF, R_b = 500 Ω, and R_m = -1 MΩ.

If you couldn't solve part (b), you can plot the transfer function:

$$\frac{V_{out,f}}{V_s} = \frac{Kw^2}{1 + jw/w_1}$$

where $K = 5 \times 10^{-16}$ s^2 and $\omega_1 = 8 \times 10^8$ rad/s.



(d) [5 pts.] If a drive voltage waveform is $v_d(t)$ = 100 mV cos[(10 Mrad/s)t] is applied to the input, what is the output voltage waveform due to feedthrough, $v_{out,f}(t)$? Use your results from parts (b) and (c), or the alternative transfer function given in part (c)