University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Midterm 1

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Problem	Points	Score
1	20	
2	40	
3	10	
4	10	
5	20	
Total	100	

- You may use a calculator
- Show all your work and reasoning on the exam in order to receive full or partial credit.
- Write your answer in the designated page for each problem. If you need more space, use the "Additional Space" at the end.
- **Please put a box around the final answer of each sub-problem**
- **Time: 90 minutes**

Please use the following parameters for all problems unless specified otherwise:
Φ_{n+} = 550 mV, Φ_{p+} = -550mV, V_{th} = 26mV
ε_{Si} = 11.7, ε_{SiO2} = 3.9, ε_0 = 8.854 x 10^{-14} F/cm,
Q = 1.6 x 10_{-19} C, n_i = 10^{10} cm^{-3}

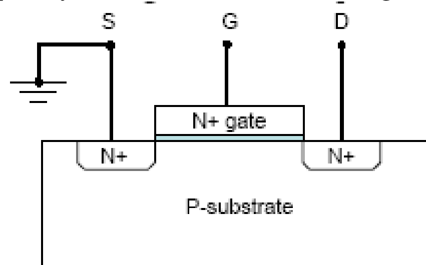
1. Consider a silicon PN junction diode with an N-doping concentration of 10^{16} cm^{-3} and a P-doping concentration of 10^{18} cm^{-3}. Their cross-sectional area of the diode is 100 um^2. Assume the reverse saturation current of the diode is 10^{-14} Amp. The diode is forward biased at 0.7V.
    a) [10pt] Find the dynamic resistance at this bias.
    b) [10pt] Find the depletion capacitance at this bias.

2. Consider a MOS capacitor with a P+ polysilicon gate and an N-doped substrate with a doping concentration of 10^{16} cm^{-3}. The thickness of the oxide is 230nm.
    a) [10pt] Find the threshold voltage.
    b) [10pt] Which mode is the MOS capacitor in when its gate is biased at 1V?
    c) [10pt] What is the maximum capacitance per unit area?
    d) [10pt] What is the minimum capacitance pr unit area?

3. [10pt] For the MOS capacitor in Problem (2), plot the charge density distribution as a function of position when the gate is biased at –2V. Please be as quantitative as possible. Show the positions of all charges, and show the magnitude and polarity of the charges.

4. [10pt] If the P+ gate of the MOS capacitor in Problem (2) is replaced by a metal whose electrostatic potential is 0V. What is the threshold boltage of the new MOS capacitor?

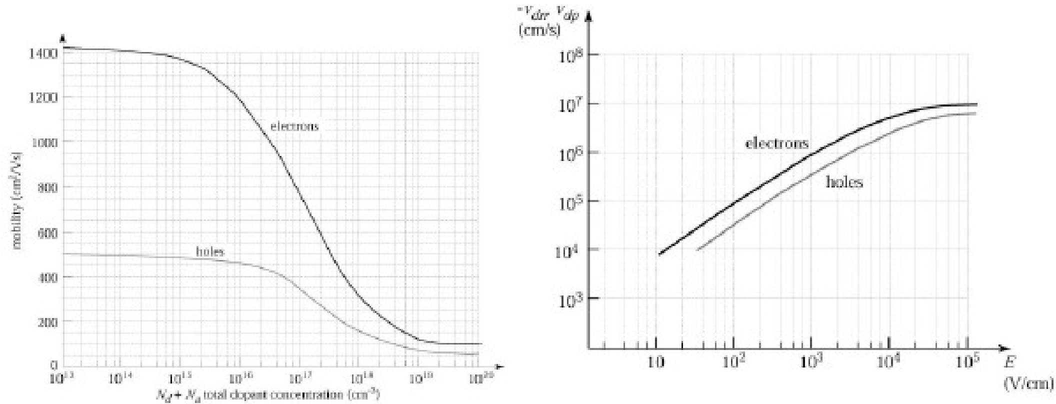
5. Consider an N-MOSFET with an N+ polysilicon gate on P-type substrate (N_a = 10^{17} cm^{-3}). The source is grounded, and the drain is biased at 5V. The transistor has a gate length of 1 um, and a width of 10 um. The thickness of the gate oxide is 10 nm. For simplicity, assume the channel-length modulation parameter λ = 0.



    a) [10pt] At what gate voltage does the transistor turn on, i.e., start to have significant current flowing between source and drain?
    b) [10pt] Find the drain current when the gate is biased at 2V.

Some equations

Mass-action law $n \times p = n_i^2(T)$



Resistivity: $\rho_n = \dfrac{1}{\sigma_n} = \dfrac{1}{q\mu_n N_{d,eff}}$

Resistance: $R = \dfrac{\rho L}{Wt} = \left(\dfrac{\rho}{t}\right)\left(\dfrac{L}{W}\right) = R_{sq}\left(\dfrac{L}{W}\right)$

Total current (e⁻): $J = J_{drift} + J_{diff} = q\mu_n nE + qD_n \dfrac{dn}{dx}$

Gauss's law: $\oint E \cdot dS = \dfrac{Q}{\varepsilon}$ $\quad Q = CV \quad$ $E = -\dfrac{d\phi}{dx}$

Depletion layer: $X_{d0} = x_{p0} + x_{n0} = \sqrt{\dfrac{2\varepsilon_s \phi_{bi}}{q}\left(\dfrac{1}{N_a} + \dfrac{1}{N_d}\right)}$ $\quad X_d(V_D) = X_{d0}\sqrt{1 - \dfrac{V_D}{\phi_{bi}}}$

pn depletion layer capacitance: $C_j = \dfrac{qN_a x_{p0}}{2\phi_{bi}\sqrt{1 - \dfrac{V_D}{\phi_{bi}}}} = \dfrac{C_{j0}}{\sqrt{1 - \dfrac{V_D}{\phi_{bi}}}}$

pn diffusion current $J^{diff} = qn_i^2\left(\dfrac{D_p}{N_d W_n} + \dfrac{D_n}{N_a W_p}\right)\left(e^{\frac{qv_D}{kT}} - 1\right)$ $\quad i_D = I_S\left(e^{\frac{qv_D}{kT}} - 1\right)$

Diffusion capacitance: $C_d = \dfrac{1}{2}\dfrac{qI_D}{kT}\tau$

Threshold voltage (NMOS)

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a\left(-2\phi_p\right)} \qquad \phi_p = -\frac{kT}{q}\ln\frac{N_a}{n_i}$$

$$V_{Tn} = V_{Tn0} + \gamma\left(\sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p}\right)$$

NMOS equations:

$$I_D = 0, \quad V_{GS} < V_{Tn}$$

$$i_D = \frac{W}{L}\mu C_{ox}\left(v_{GS} - V_{Tn} - \frac{v_{DS}}{2}\right)v_{DS}\left(1+\lambda V_{DS}\right), \quad V_{GS} > V_{Tn},\ V_{DS} < V_{GS} - V_{Tn}$$

$$i_D = \frac{W}{L}\frac{\mu C_{ox}}{2}\left(v_{GS} - V_{Tn}\right)^2\left(1+\lambda V_{DS}\right), \quad V_{GS} > V_{Tn},\ V_{DS} > V_{GS} - V_{Tn}$$

MOS capacitances in saturation $\quad C_{gs} = (2/3)WLC_{ox} + C_{ov} \qquad C_{ov} = L_D W C_{ox}$

MOS signal parameters:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)\left(1+\lambda V_{DS}\right) \approx \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)$$

$$r_o = \left(\left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\right)^{-1} \approx \frac{1}{\lambda I_{DS}}$$

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \frac{\gamma g_m}{2\sqrt{-V_{BS} - 2\phi_p}}$$