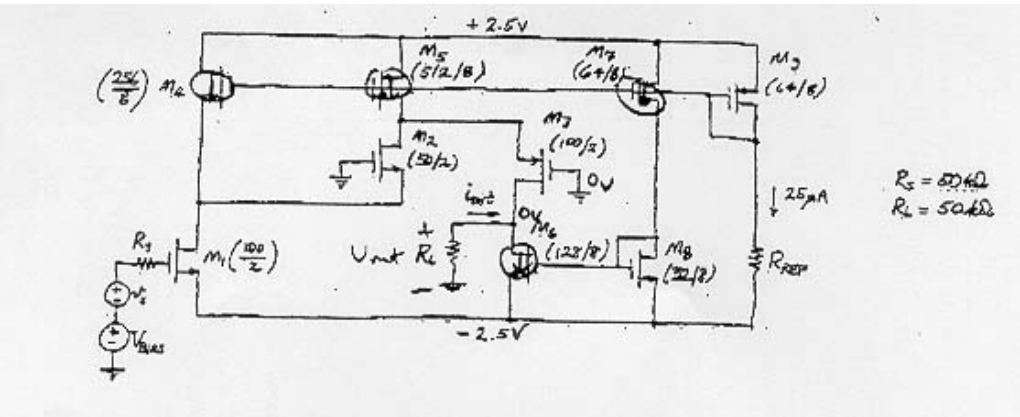
EECS 105 Spring 1998 Final

1. CMOS Transconductance Amplifier [35 pt]



(a) [3 pts] Find the numerical value of R

REF.

(b) [3 pts] Redraw the circuit with all currents supplies replaced by symbols.

(c) [3 pts] Find the numerical values of the DC currents and voltages listed in the table below.

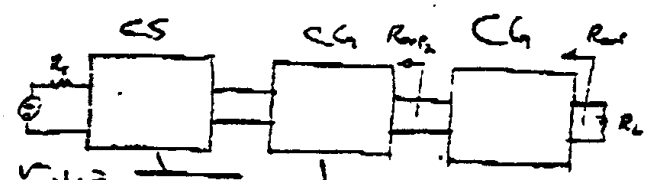
Note that V

BIAS is selected such that VOUT = 0V.

M1	I D1	V
M 2	I D2	
M 3	I D3	

(d) [4 pts] This three-stage amplifier can be modeled as the cascade below. Find the numerical value of R

OUT, 2. Answers within ±5% of the correct answer will receive full credit.



(e) [4 pts] Find the numerical value of the output resistance R

OUT. Answers within ±5% of the correct answer will receive full credit.

(f) [5 pts] Find the numerical value of the overall transconductance of the amplifier, *i*

OUT/vS,

including the effects of RS and RL the values of which are both 50 kΩROUT, 2.

Answers within ±5% of the correct answer will receive full credit.

(g) [5 pts] Find the maximum value of the output current $i_{OUT,\,max}$ for which all transistors remain in their constant-current regions. (Note that "maximum" means "most positive" in this case.)

(h) [4 pts] Find the minimum value of the output current $i_{OUT,\,min}$ for which all transistors remain in their constant-current regions. (Note that "minimum" means "most

negative" in this case.)

i. [4 pts] On the graph below, sketch i_{OUT} versus v_S. Your plot should incude the limits to i_{OUT} that you found in parts (g) and (h). If you couldnt solve these parts, you can

assume that $i_{OUT,\,max}$ =70 μA and $i_{OUT,\,min}$ = -100 μA

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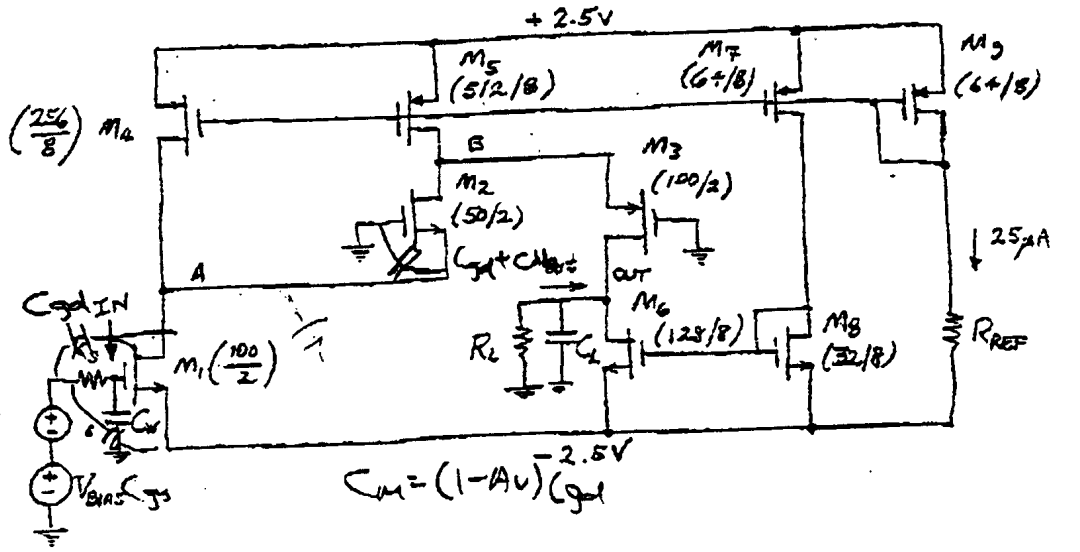
2. Frequency Response of CMOS Transconductance Amplifier



Note that a wiring capacitance C

W = 50 fF and a load capacitance CL = 500 fF have

Been added to the schematic.

a. [5 pts] Find the open-circuit time constant for the capacitance between node "IN" and ground. Use the Miller theorem to transform any capacitance connected from "IN" to another node into an equivalent capacitance to ground. Answers within ±5% of the correct answer will receive full credit.

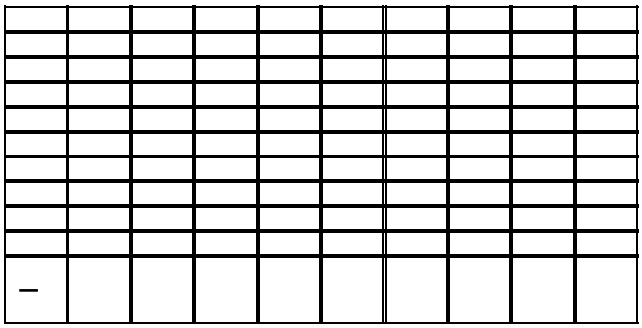
(b) [5 pts] Find the open-circuit time constant for the capacitance between node "A" and ground. Use the Miller theorem to transform any capacitance connected from "A" to another node into an equivalent capacitance to ground. Answers within ±5% of the correct answer will receive full credit.

(c) [5 pts] Find the open-circuit time constant for the capacitance between node "B" and ground. Use the Miller theorem to transform any capacitance connected from "B" to another node into an equivalent capacitance to ground. Answers within ±5% of the correct answer will receive full credit.

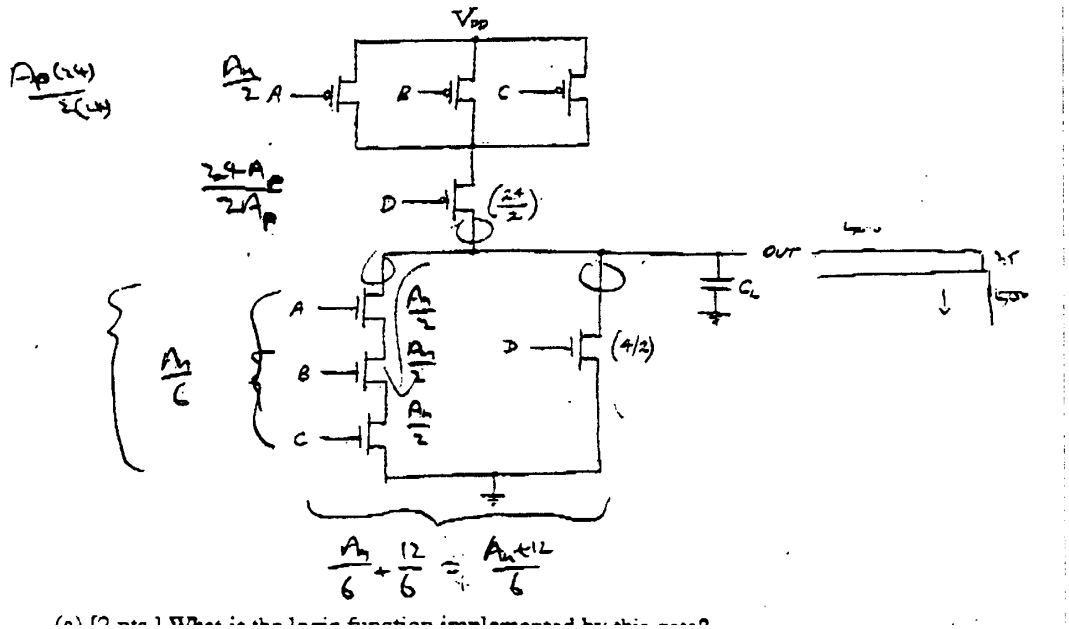
d. [5 pts.] Find the open-circuit time constant for the capacitance between node "OUT" and ground. Use the Miller theorem to transform any capacitance connected from "OUT" to another node into an equivalent capacitance to ground. Answers within ±5% of the correct answer will receive full credit.

(e) [4 pts] What is the 3 dB frequency f_1 of this amplifier in MHz, according to the open-circuit time constant approximation? Answers within ±5% of the correct answer will receive full credit. Note that you need not have done (a), (b), (c), and (d) in order to answer this part with adequate precision.

- [6 pts] SPICE simulation shows that the next pole is located at f_2 = 50 MHz. Plot the transfer function I_{OUT}/V_S on the graphs below. Note that the units of the gain will be "20 log Siemans". If you couldnt solve part (d), you can assume that f_1 = 2 MHz for this part. Also, if you couldnt solve (f), you can assume that I_{OUT}/V_S= 0.5 mS for this part.



3. CMOS Digital Gate [20 pts]



[2 pts] What is the logic function implemented by this gate?

(b) [3 pts] Find the widths of NMOS transistors A, B, and C such that the hig-to-low propagation delay t_{PHL} is the same as the slowest t

$_{PHL}$. Given: $W_{An} = W_{Bn} = W_{Cn}$ abd all transistors have the same gate length L= 2μm

c. [3 pts.] Find the widths of PMOS transistors A, B, and C such that the worst-case low-to-high propagation delay is equal to the high-to-low propagation delay: t

PLH, wc = tPHL. Given: $W_{An} = W_{Bn} = W_{Cn}$ abd all transistors have the same gate length L= 2μm.

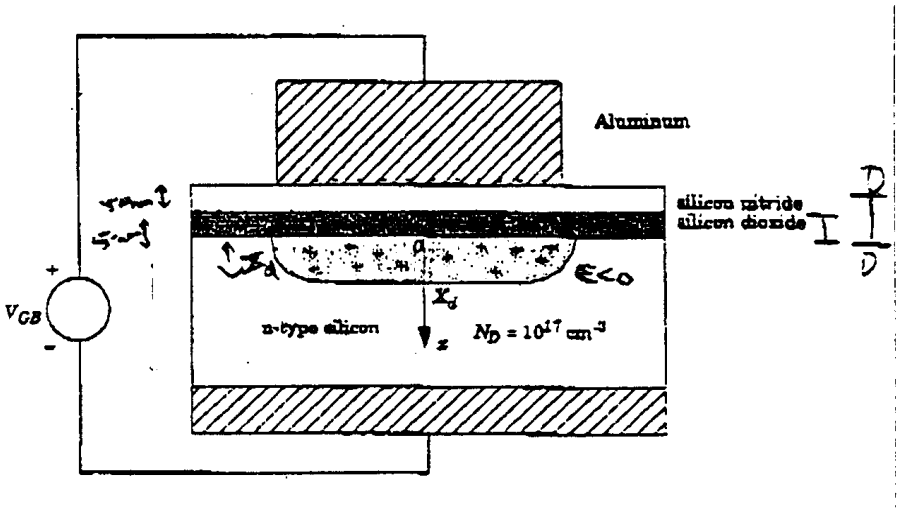
d. [3 pts] Find the numerical value of C

DB for this gate in fF.

- [3 pts.] The aluminum line from the output to the next gate is 500 µm Iin the length and 2.5µm wide. Given that the field oxide under the aluminum is 500 nm in thickness, find the numerical value of the wire capacitance Cw.

- [3 pts.] Find the max fanout of this logic gate, assuming that the ouput is connected to one input of each of the CMOS gates and that the transistors in these "load gates" have dimensions: PMOS: (W/L)= 20/2 and NMOS: (W/L) = 10/2. The propagation delay must be less than 15 ns. If you couldnt get parts (d) and (e), you can assume that C
  $_{DB}$=200 fF and that C$_{W}$ = 150 fF

- [3 pt] Estimate the minimum supply voltage V
  DD for which the noise margins of this logic gat will be greater than 500mV



4. MOSE Electrostatics [15 pts]

Given: Permittivities ε(silicon) = 11.7 ε0 (silicon, Xd= -750 A= 75 nm)

ε(oxide) = 3.9 ε0 (silicon dioxide) thickness; t=500A= 50nm

ε(silicon nitride) = 7.5 ε0 (silicon nitride) thickness; t=50nm

a. [4pts] Find the numerical value of the electric field E(x=0+), which is just inside the silicon.

b. [3 pts] Find the numerical value of the electric field E(x=0-), which is just inside the silicon dioxide. If you couldnt solve (a), assume E(x=0+)= 50kV/cm.

c. [4 pts] Find the numerical value of the potential drop across the oxide/nitride sandwich. You can make the same assumption as in (b) as a default.

(d) [4 pts] Finf the numerical value of the capacitance C_{gb} for the MOS capacitor biased as shown in the figure.