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UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences
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Test #2

1) You have been asked to implement a digital thermometer based on a one-sided P^+N junction temperature sensor. The thermometer is intended for use around room temperature or so.

   a) Do you expect the following I_0-related parameters to increase or decrease with temperature?

      i) n_i: *will increase, due to increased thermal generation*

      ii) D: *will probably decrease slightly (see test 1 solutions)*

      iii) L: *will probably decrease slightly, as above.*

3 pts

   b) Based on your answers above, do you expect I_0 to increase or decrease with temperature? Give reasons.

2 pts

I_0 will increase, since n_i increases very strongly, unlike the decreasing parameters.

   c) Suppose I were to ignore the effect of T on I_0, would I expect the on-current at a given bias voltage to increase or decrease with temperature? Give reasons

1 pt

The kT in the exponent would cause current to decrease.

   d) In general, at low bias voltages, the on-current is found increase with temperature, while it decreases with temperature at higher voltages. Explain the reason for this.

2 pts

At low biases, I_0 dominates, so current increases. At high biases, the exponent dominates, so current decreases.

2) In this question, we will consider the effect of high forward bias voltages on our diode analysis.

   a) The low-level injection assumption states that the concentration of minority carriers injected is substantially less than the majority carrier concentration. This assumption breaks down at high voltages. What is the consequence of this on the mechanisms of majority carrier current flow (in other words, on drift and diffusion of the majority carriers)?

2 pts

If minority carrier concentration isn't negligible, then majority carriers must also increase to ensure charge neutrality. This will result in an increase in majority carrier diffusion relative to drift.

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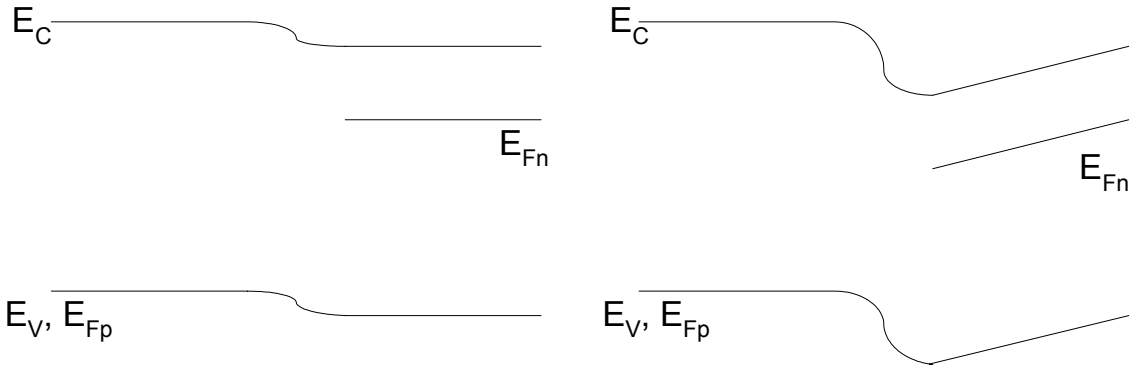
b) Our W_{dep} equations predict that W_{dep} becomes imaginary as V_{diode} exceeds V_{bi}. Obviously, this isn't correct. In reality, series resistance becomes dominant long before V_{diode} even approaches V_{bi}, and most of the voltage is dropped as series resistance.

5 pts

Assume that $V_{bi} = 0.8V$. Draw 2 band diagrams for a P^+N diode at $V_{diode} = 0.7V$. In the first diagram, assume that series resistance is ignored. In the second diagram, assume 0.2V is dropped as series resistance (HINT: think about which region is likely to have the most series resistance when you draw the 2nd band diagram, and remember that regions without any net space charge cannot have any curvature in the band structure)



3) Germanium is considered a promising material for use in future semiconductor circuits, primarily due to its high mobility. Unfortunately, it suffers from several problems in PN diode applications. Compare Ge diodes to similarly structured and doped Si diodes for the following (give reasons):

a) Leakage current

Ge diodes will have much larger leakage, due to a larger n_i and therefore large I_0

2 pts

b) Avalanche breakdown

Ge diodes will suffer from avalanche at lower voltages, due to increased impact ionization. Since the bandgap is smaller, less energy is required to cause impact ionization.

c) Built-in voltage

Built-in voltage will generally be lower, since the bandgap is smaller. Obviously, the built-in voltage cannot exceed the bandgap.

d) Series resistance

Series resistance for Ge diodes will probably be lower due to the increases mobility, resulting in smaller resistivity for a given doping.

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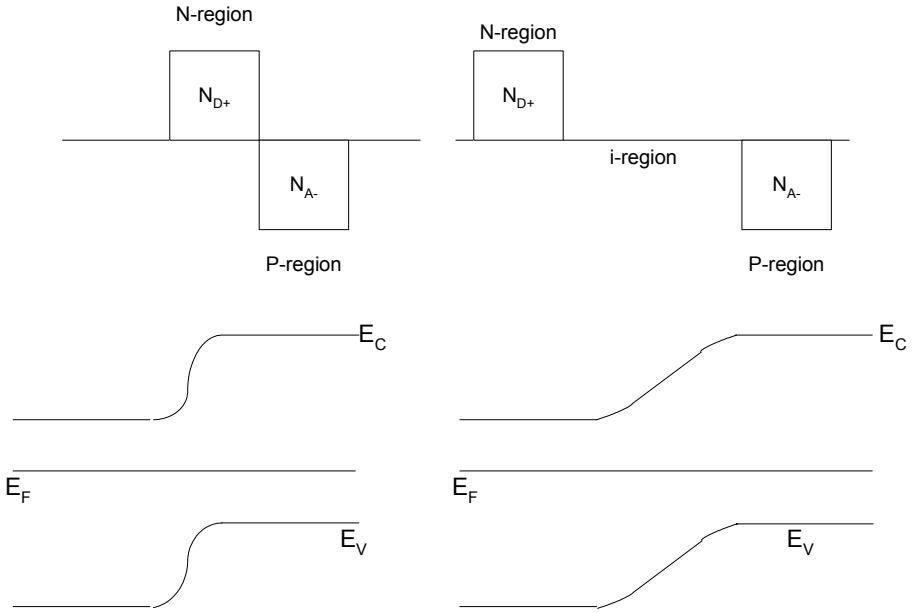
4) A PIN diode is a PN diode with an intrinsic region inserted into the depletion region.

a) Remembering that there is no space charge in the intrinsic region (since it has no ionized donors and acceptors), draw band diagrams for a PN junction and a PIN junction with identical doping. Assume that the I-region is exactly the same thickness as W_{dep} in the PN junction. As a hint, the space charge profile for the PN and PIN junctions are shown below.

5 pts



b) As you will see in your next class, PIN junctions are commonly used in photodetectors. Aside from this application, PIN diodes are also popular for use in high-speed circuits, since the typically show faster switching response than equivalent PN diodes. Why is this true? To justify your answer, derive an equation for the C-V characteristics of a PIN diode, and contrast it to a PN diode.

3 pts

Since the i-region is undoped, the next length of W_{dep} is increased. This decreases the depletion capacitance, which, in turn, increases the switching speed. For a PN junction, the depletion capacitance is: $C_{dep} = \frac{\varepsilon \cdot A}{x_n + x_p}$, *where x_n and x_p are the extents of the depletion region in the p and n regions respectively. For a PIN junction, the depletion capacitance is:* $C_{dep} = \frac{\varepsilon \cdot A}{x_n + x_p + W_i}$, *where W_i is the additional length added by the i-region. Thus, the net capacitance is smaller, resulting in higher speed.*