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UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences
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Final Examination

1) Solar cells are often built in amorphous silicon, which has a very short recombination lifetime and low diffusion coefficient. Consider a solar cell illuminated through a window such that only a small section of the device receives light. The window is moved from one end of the device to the other.

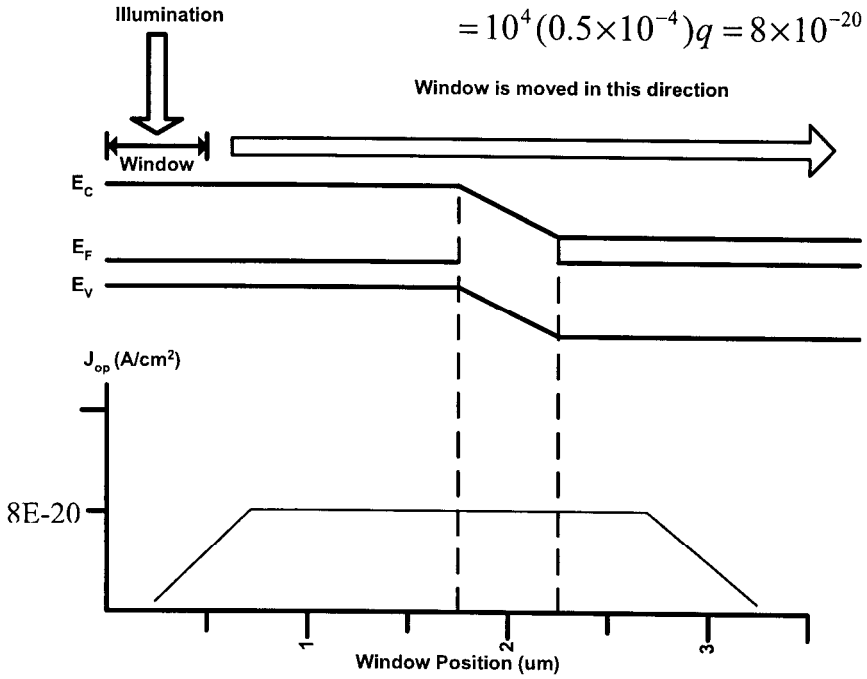
a) Calculate and plot the short-circuit current density as a function of window position (defined as the position of the left edge of the window). You may assume that only and all excess carriers generated within a diffusion length of the depletion region contribute to current flow.

τ for all carriers = 10^{-7} sec
D for all carriers = 0.1 $cm^2 sec^{-1}$
$g_{op} = 10^4$ cm^{-3} sec^{-1}

$$L = \sqrt{0.1\times10^{-7}} = 1\mu m$$

$$J_{op\max} = qg_{op}(W_{window})$$

$$= 10^4(0.5\times10^{-4})q = 8\times10^{-20}\,A/cm^2$$



b) In general, amorphous silicon solar cells produce much lower current than similarly sized solar cells made of single crystal silicon. Why?

The reduced carrier lifetime and diffusivity greatly reduces the region in which carriers are generated.

c) Silicon is widely used in solar cells, but has not been used to make LEDs. Why?

Silicon is an indirect semiconductor with a bandgap in the infrared, so direct recombination in the visible spectrum is not possible. Hence, production of visible light is not possible.

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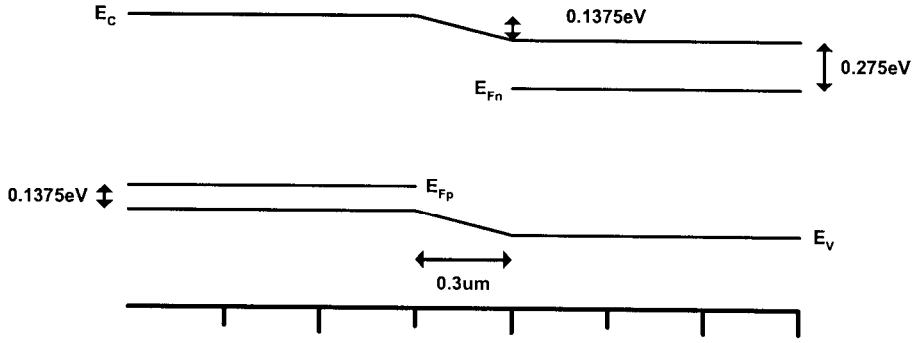
2) Consider the silicon P^+N junction below (E_G=1.1eV).



a) What is the voltage on the device?

0.55V, calculated from the energy distance between the quasi-fermi levels.

b) What is the capacitance of the device?

$$C_{dep} = A\frac{\varepsilon_s}{W_{dep}} = A\frac{11.7\times8.85\times10^{-14}}{0.3\times10^{-4}} = 34nF/cm^2$$

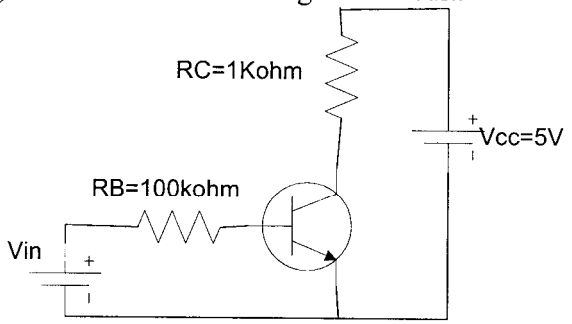
c) If the n-side is doped to 1E17, what is the minority carrier concentration at the edge of the depletion region (assume $n_i = 10^{10}cm^{-3}$)?

$$p_n = p_{n0}(e^{qV/kT}) = \frac{10^{20}}{10^{17}}(e^{0.55/0.026}) = 1.5\times10^{12}/cm^3$$

d) Calculate the diode current density ($D_p = 10cm^2/sec$)

$$J = qD_p\frac{dp}{dx} = 1.6\times10^{-19}\cdot10\cdot\frac{5\times10^{19}-10^3}{0.9\times10^{-4}} = 27mA/cm^2$$

3) Consider the following BJT circuit.



$D_E = 2cm^2/sec$
$D_B = 10cm^2/sec$
$N_B = 5E17cm^{-3}$
$N_E = 1E19cm^{-3}$
$\tau = 10^{-5}$ sec
$W_E = 0.2um$
$W_B = 0.2um$

a) What is the gain of the transistor? Ignore base-width modulation and emitter bandgap narrowing. You may should the short-base assumption throughout

$$\beta_{dc} = \frac{1}{\frac{D_E}{D_B}\frac{N_B}{N_E}\frac{W}{W_E} + \frac{1}{2}\left(\frac{W}{L_B}\right)^2} = \frac{1}{\frac{2}{10}\frac{5E17}{1E19}\frac{0.2}{0.2} + \frac{1}{2}\left(\frac{0.2\times10^{-4}}{0.01}\right)^2} = 100$$

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b) Assume $I_B = (V_{IN}-0.6V)/R_B$ for Vin>0.6V. Calculate the voltage at the collector when
i) Vin=0V
$V_{collector} = 5V \text{ since } I_C = 100*I_B = 0V$

ii) Vin=1V
$V_{collector} = 5V - 1K*100*I_B = 5\text{-}1K*100*0.4/100K=4.6V$

iii) Vin=2V.
$V_{collector} = 5V - 1K*100*I_B = 5\text{-}1K*100*1.4/100K=3.6V$

c) What type of digital logic element does this circuit represent?
This is an inverting function.

d) At Vin=2V, calculate the transconductance and small signal input resistance of the BJT.

$$g_m = \frac{I_C}{kT/q} = \frac{100 \cdot 1.4/100K}{0.026} = 0.054S$$

$$r_\pi = \frac{\beta_F}{g_m} = \frac{100}{0.054} = 1.8K\Omega$$

4) You are designing an output stage that is supposed to run at extremely high power.

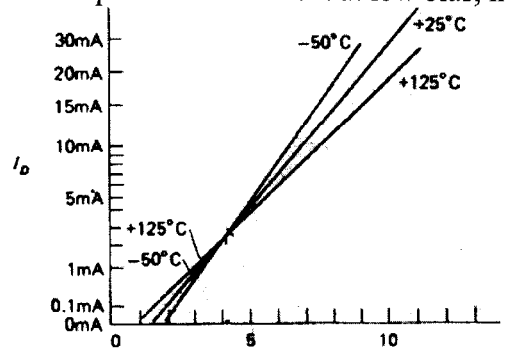
a) What is the effect of increased temperature on BJT gain?
The gain of a BJT increases with increasing temperature (causing the thermal runaway effect)

b) What is the effect of increased temperature on the following parameters in a MOSFET?
i) Surface mobility
Mobility decreases with increasing temperature due to increased phonon scattering.

ii) Oxide capacitance
Oxide capacitance does not change with temperature to first order

iii) Theshold voltage
Threshold voltage drops slightly with temperature.

c) The variation in the I_D-V_G curves for a MOSFET as a function of temperature is shown below. What causes the change in temperature coefficient as a function of gate bias (i.e., positive coefficient at low bias, negative coefficient at high bias)?



The negative temperature coefficient at high bias is due to the reduction in mobility with temperature. At low bias, where current is mainly limited by threshold voltage, the temperature coefficient is positive due to the reduction in threshold voltage with temperature. These two effects together cause the variation in temperature coefficient with bias.

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d) Would you choose to use BJT's or MOSFET's based on heat considerations? Why?
A MOSFET would be the obvious choice due to the absence of thermal runaway effects, since the MOSFET is a negative temperature coefficient device at high currents. BJTs are not preferred since they are prone to thermal runaway.

5) The contact formed between metals and silicon is important since it enables interconnection of devices in circuits. In particular, formation of low resistance ohmic contacts is required.

a) What is the requirement placed on the workfunction of a metal that is to be used in forming an ohmic contact to n-type silicon doped to 1E17 (Workfunction ~4.15eV)?
The workfunction of the metal must be less than 4.15eV, such insignificant barrier to electron flow is present.

b) What is the requirement placed on the doping concentration of n-type silicon (Electron Affinity ~4.05eV) that is to be used in forming an ohmic contact to Gold (Workfunction ~5.1eV)?
The silicon must be heavily doped (typically greater than 5E19) such that a tunneling contact is formed.

c) You are required to form a low-resistance contact from W (Workfunction ~4.6eV) to n-type silicon. Calculate the minimum doping level required to form such a contact if tunneling is only appreciable for barriers less than 50 Angstroms thick. You may use the foreknowledge that the silicon will be heavily doped to simplify your solution

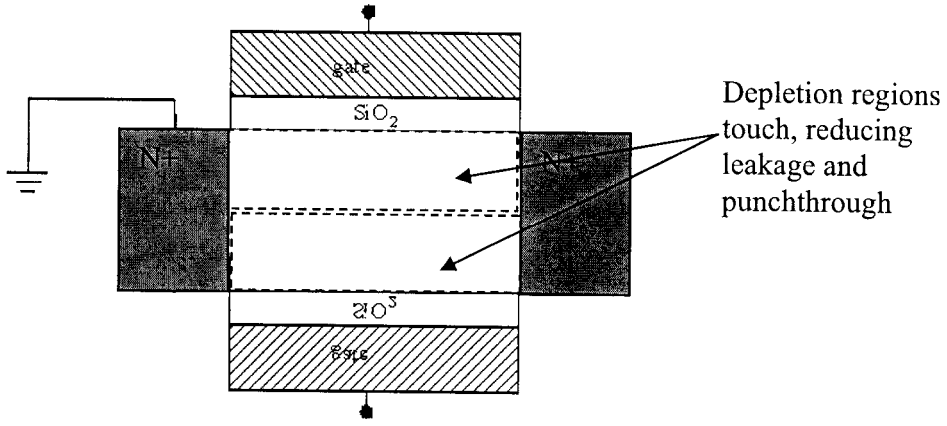
Since the silicon is heavily doped, assume that $\phi_i = \Phi_M - X_{Si}$

Now, the depletion width is: $W_{dep} = \sqrt{\frac{2\varepsilon_s \phi_i}{qN_d}}$

Solving for N_d*, we have:* $N_d = \frac{2\varepsilon_s \phi_i}{W_{dep}^{\ 2} q}$

For W_{dep} *= 50 Angstroms,* $N_d \sim 3E19\ cm^{-3}$.

6) The double-gate MOSFET is a promising structure for future generations of circuits. The classic double gate MOSFET uses two gates placed such that their depletion regions touch, resulting in substantially improved leakage and punchthrough resistance.



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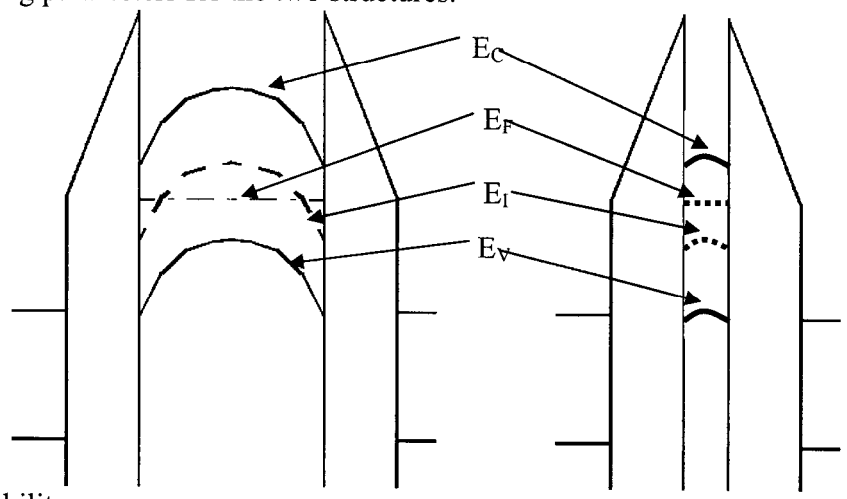
a) For a gate oxide thickness of 30 Angstroms and a body doping of 1E17cm^{-3} Boron, calculate the body thickness such that the body is fully depleted, i.e., the two depletion regions touch when the MOSFET is at threshold. Assume both gates are n-type polysilicon.

$$\phi_B(N) := \frac{k \cdot T}{q} \ln\left(\frac{N}{n_i}\right) \qquad \phi_S(N) := 2 \cdot \phi_B(N)$$

$$x_{dmax}(N) := \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot \varepsilon_0 \cdot \phi_S(N)}{q \cdot N}} \qquad x_{dmax}\left(10^{17} \cdot cm^{-3}\right) = 0.104\,\mu m$$

$$t_{body} := 2 \cdot x_{dmax}\left(10^{17} \cdot cm^{-3}\right) \qquad t_{body} = 0.209\,\mu m$$

b) A more recent development has been the ultra-thin body (UTB) double gate MOSFET, in which the body is thinned so much that the depletion regions are non-existent, and the inversion layers of the two channels touch. The respective band profiles for the classic and UTB double gate devices are shown below (note that the body potential in the UTB device is raised by the interaction between the two inversion layers). Compare the following parameters for the two structures.



i) Mobility

The UTB structure should have a higher mobility due to the reduced transverse electric field.

ii) Leakage

The UTB structure should have lower leakage due to reduced cross-sectional area available to serve as a leakage path.

iii) Series Resistance

The UTB structure should have a higher series resistance due to the reduced cross-sectional area of the channel and hence the source / drain.

iv) Overlap capacitances

The overlap capacitances for the two structures should be similar.

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7) Parasitic resistance is a serious problem in modern MOSFETs. Consider a MOSFET that is misfabricated such that one side of the MOSFET has a 100Ω parasitic resistor in series with it. You may place the device such that the resistor is at the source or drain.

a) Calculate and compare the on-current ($V_D = V_G = V_{DD}$, $V_S = 0V$) for the two configurations, as well as for an ideal MOSFET with no parasitic resistance. You may make approximations where appropriate. You are given the following parameters:

$V_{DD} = 2.5V$
$V_T = 0.5V$
$L = 0.2um$
$W = 0.4um$
$\mu = 400cm^2V^{-1}s^{-1}$
$t_{ox} = 3nm$

The device is in saturation, based on the bias conditions. Therefore:
When the resistor is at the drain, we have:

$$I_{D\_drain} := \frac{\mu \cdot C_{ox} \cdot W}{2 \cdot L} \cdot (V_{DD} - V_T)^2$$

$$I_{D\_drain} = 1.841 \cdot mA$$

When the resistor is at the source, we have to solve iteratively. If we use the number above as the first guess, we have:

$$I_{D\_source\_approx} := \frac{\mu \cdot C_{ox} \cdot W}{2 \cdot L} \cdot (V_{DD} - 100\Omega \cdot I_{D\_source\_guess} - V_T)^2$$

$$I_{D\_source\_approx} = 1.518 \cdot mA$$

Plugging this number back in, and re-solving, we obtain 1.572mA, which suggests that the answer is approx. 1.5mA.

b) Based on your results, comment on the importance of parasitic resistance in the source and drain.

The effect of the resistor in the source is significant (approx 20% decrease in current) while the resistor in the drain has no effect on saturation current.

c) Will your analysis change were the device biased in the linear region? Why?

In the linear region, we would expect the drain resistor to have an effect on current as well, since the on-current in the linear region depends on V_{DS}, which will be reduced by voltage drop across the drain resistor.

8) You are working with two novel semiconductors. Material "A" has a saturation velocity of 10^7cm/s and a mobility of $500cm^2V^{-1}s^{-1}$. Material "B" has a saturation velocity of 10^6cm/s and a mobility of $2000cm^2V^{-1}s^{-1}$.

a) What is the saturation field for the two materials?

$$\varepsilon_{sat\_A} := \frac{v_{sat\_A} \cdot 2}{\mu_A} \qquad \varepsilon_{sat\_B} := \frac{v_{sat\_B} \cdot 2}{\mu_B}$$

$$\varepsilon_{sat\_A} = 4 \cdot 10^4 \cdot \frac{V}{cm} \qquad \varepsilon_{sat\_B} = 1 \cdot 10^3 \cdot \frac{V}{cm}$$

b) Suppose the long-channel I_{Dsat} for a MOSFET made with material "A" is 400μA, what is the long channel I_{Dsat} for a MOSFET made with material "B"?

$$I_{Dsat\_B} := I_{Dsat\_A} \cdot \frac{\mu_B}{\mu_A} \qquad I_{Dsat\_B} = 1.6 \cdot mA$$

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c) What are the I_{Dsat}'s for 0.2μm MOSFETs fabricated with the two materials given a supply voltage of 2.5V? Use the following equation to find your solution: $I_{Dsat} = \frac{I_{Dsat\_Long}}{1+V_{DS}/\varepsilon_{sat}L}$

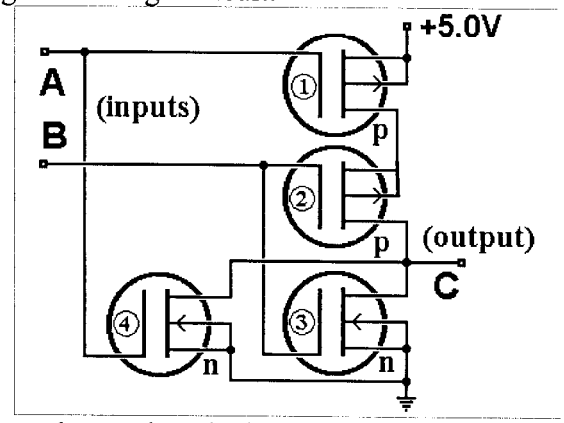
$$I_{Dsat\_0.5\_A} := \frac{I_{Dsat\_A}}{1+\frac{2.5\cdot volt}{\varepsilon_{sat\_A}\cdot 0.2\cdot\mu m}} \qquad I_{Dsat\_0.5\_B} := \frac{I_{Dsat\_B}}{1+\frac{2.5\cdot volt}{\varepsilon_{sat\_B}\cdot 0.2\cdot\mu m}}$$

$I_{Dsat\_0.5\_A} = 96.97\cdot\mu A$ $\qquad$ $I_{Dsat\_0.5\_B} = 12.698\cdot\mu A$

d) Based on your results in (b) and (c) above, comment on the relative importance of mobility and saturation velocity in long and short channel MOSFETs. Give reasons. Consider the effect of the regions of operation, i.e., linear vs. saturation.

Mobility is important in long-channel MOSFETs, since the MOSFET operates outside the velocity saturation regime. On the other hand, short-channel MOSFETs operate in the velocity saturation region, so the saturation velocity is often more important that the mobility, at least from a drive-current consideration in saturation. In the linear regime, short-channel MOSFETs still depend more heavily on mobility, since the lateral field is small.

9) Consider the following CMOS logic circuit:



a) Estimate the output voltage when the input voltages are:
   i) A = 0V, B = 0V, Out = 5V
   ii) A = 0V, B = 5V, Out = 0V
   iii) A = 5V, B = 0V, Out = 0V
   iv) A = 5V, B = 5V, Out = 0V

b) Choose the PMOSFET width (same for both devices) such that Vout = 2.5V when VA = VB = 2.5V. You are given the following information:

$W_{NMOS} = 0.5um$
$L_{NMOS} = L_{PMOS} = 0.25um$
$\mu_{NMOS} = 2\mu_{PMOS}$

Since the two PMOS devices are in series, we can effectively model them as one PMOS of twice the L. Therefore, we should choose use PMOS transistors with W=4.0μm to maintain the same uW/L ratio as the NMOS (which has an effective W/L=1/0.25)

c) Now, suppose the body of MOSFET#2 is connected to Vdd rather than to the source of #2. Will the switchover input voltage in (b) increase or decrease? Why?

If the body of MOSFET#2 is connected to Vdd, its threshold voltage will increase due to the body effect. As a result, the current through the PMOS chain will decrease. This will result in an increased effective resistance of the PMOS chain. The NMOS effective resistance will be unchanged, resulting in a decrease in the output voltage for a given input voltage. Therefore, the switchover voltage (i.e, the input voltage at which the output is at 2.5V) will decrease.

10) Consider a 0.2μm CMOS technology with the following specifications:

T_{ox} = 2.5nm
$N_{surface}$ = 1E17cm^{-3} (used to control threshold voltage)
N_{halo} = 1E18 cm^{-3}
$N_{S/D}$ = 1E20 cm^{-3}
$N_{extension}$ = 1E19 cm^{-3}
r_j = 0.15μm

Explain the effect of the following process changes on drive current and leakage current. Give reasons for your answers.

a) The surface doping is decreased due to a processing mistake. To correct for this, the designer increases the oxide thickness to keep the threshold voltage the same.

Drain-induced barrier lowering will increase, resulting in more leakage current. The drive current will be decreased due to the lower capacitance (note: mobility will increase, but not as much.)

b) The junction depth of the extension is increased due to a processing mistake. The increase in the junction depth is radially symmetric.

The leakage current will increase due to reduced V_T (caused by increased rolloff) and L. The drive current will be increased due to decreased L and V_T as well.

c) The junction depth of the extension is increased due to a processing mistake. The increase in the junction depth is vertical only.

The leakage current will increase due to reduced V_T (caused by increased rolloff). The drive current will increase due to the reduced V_T.

d) The Halo implant is shallower than intended due to a processing error.

The threshold voltage will increase due to more body doping. This will reduce leakage and drive current.

e) The doping in the source and drain is less than planned due to a processing error.

The series resistance in the source and drain will increase. This will cause voltage drop when current flows, reducing both leakage and drive current.