UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

FINAL EXAMINATION 2
EE 130/230A: Spring 2015
Time allotted: 90 minutes

NAME: _____ Solution

STUDENT ID#: _____

INSTRUCTIONS:

1. **Unless otherwise stated, assume**
   a. **temperature is 300 K**
   b. **material is Si**

2. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
   - Specially, while using chart, make sure that you indicate how you have got your numbers. For example, if reading off mobility, clearly write down what doping density that corresponds to.
   - Clearly write down any assumption that you have made.
- **Clearly mark (underline or box) your answers.**
3. **Specify the units on answers whenever appropriate.**

SCORE: 1 _____ **/ 20**

2 _____ **/ 20**

3 _____ **/ 20**

Total _____ **/ 60**

PHYSICAL CONSTANTS

Description	Symbol	Value
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.026 V

PROPERTIES OF SILICON AT 300K

Description	Symbol	Value
Band gap energy	E_G	1.12 eV
Intrinsic carrier concentration	n_i	10^{10} cm^{-3}
Dielectric permittivity	ε_{Si}	1.0×10^{-12} F/cm

USEFUL NUMBERS

$V_T \ln(10) = 0.060$ V at T=300K

Depletion region Width:

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)\left(V_{bi}-V_{Applied}\right)}$$

Current in a PN junction:

$$I = A\left(q\frac{D_p}{L_p}p_{n0}+q\frac{D_n}{L_n}n_{p0}\right)\left(e^{qV_D/kT}-1\right)$$

Electron and Hole Mobilities in Silicon at 300K

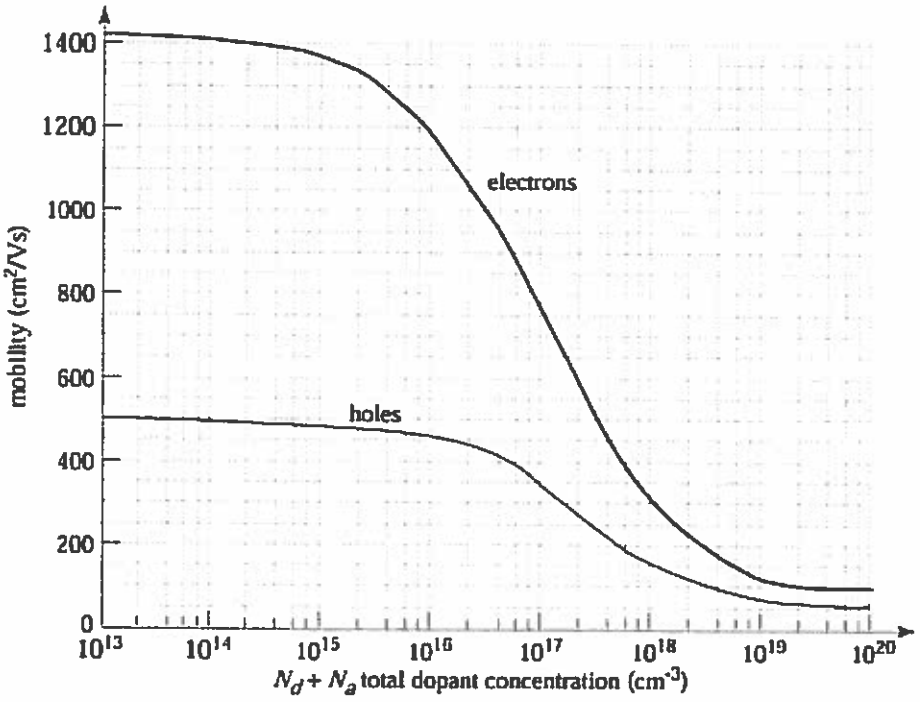


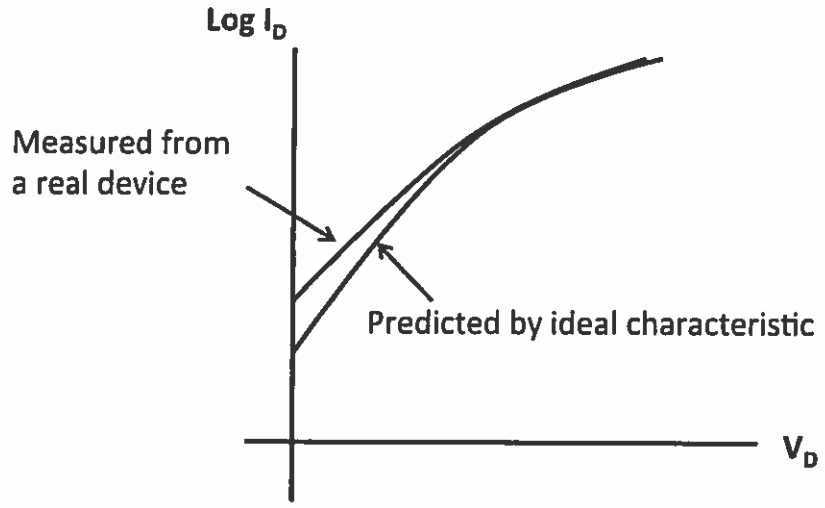
Table1: Barrier Heights of Different Metals to Si

Metal	Mg	Ti	Cr	Ni	W	Mo	Pd	Au	Pt
ϕ_{Bn} (V)	0.4	0.5	0.61	0.61	0.67	0.68	0.77	0.8	0.9
ϕ_{Bp} (V)		0.61	0.5	0.51		0.42		0.3	
Work Function ψ_m (V)	3.7	4.3	4.5	4.7	4.6	4.6	5.1	5.1	5.7

Table 2:Barriet Heights of Different Silicide Alloys to Si

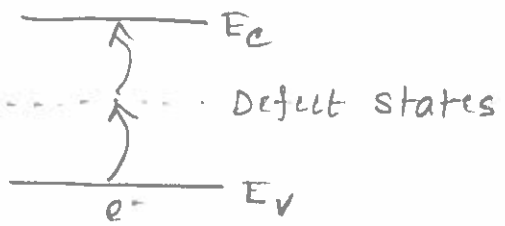
Silicide	$ErSi_{1.7}$	HfSi	$MoSi_2$	$ZrSi_2$	$TiSi_2$	$CoSi_2$	WSi_2	$NiSi_2$	Pd_2Si	PtSi
ϕ_{Bn} (V)	0.28	0.45	0.55	0.55	0.61	0.65	0.67	0.67	0.75	0.87
ϕ_{Bp} (V)		0.45	0.55	0.49	0.45	0.45	0.43	0.43	0.35	0.23

Problem 1.a [10 pts] Consider a Si-diode for which I-V characteristic is shown in the following. The measurement is done at room temperature. A discrepancy from the ideal characteristic is seen such that an increased OFF current is observed.



I. [4 pts] What is the likely reason behind the discrepancy between the ideal and measured characteristic? Clearly explain.

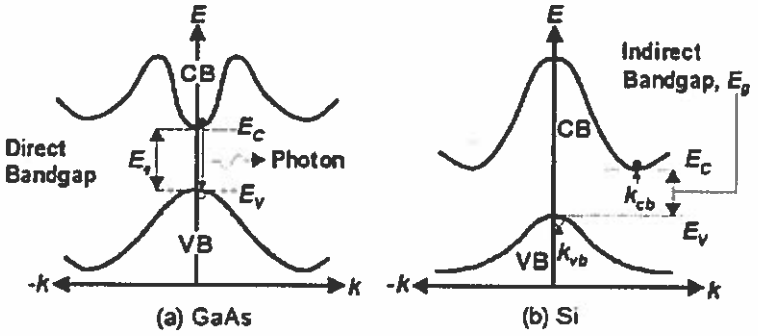
The most likely reason is junction leakage that happens due to defects which introduce states in the bandgap. Electrons can go to the E_c from E_v through defect states as shown in the figure. These additional electrons lead to increased current at the OFF state.



II. [3 pts] Will the discrepancy change at elevated temperature? If yes, will it go up or down? Why?

The discrepancy will go up at elevated temp as electrons will have more thermal energy to jump to E_c from E_v.

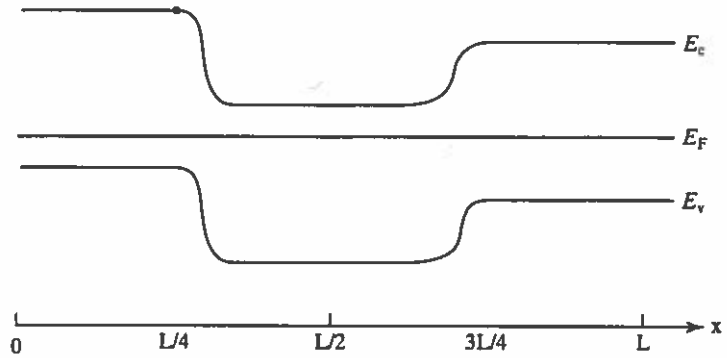
III. [3 pts] Based on the following bandstructure for Si and GaAs, which material will give higher OFF current? Why?



GaAs → because it is a direct bandgap material, so electrons do not need to change k to go to E_c from E_v.

Prob 1b. [10 pts]

A silicon sample is characterized by the energy band diagram in the following figure:

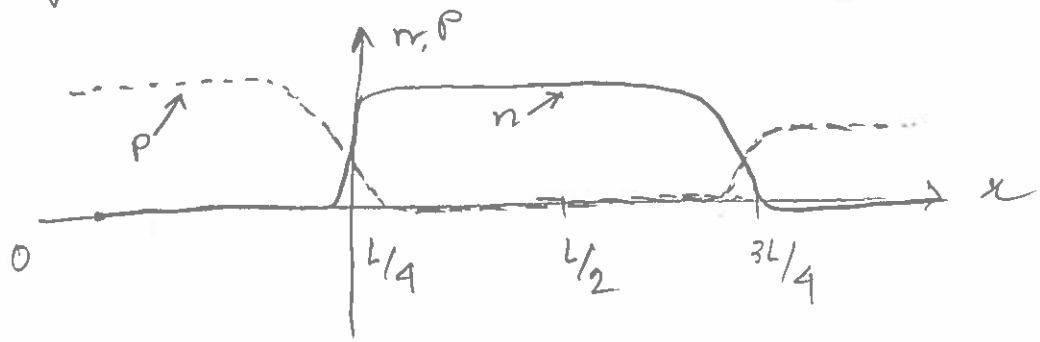


i. [2.5 pts] What kind of transistor is it?
ii. [2.5 pts] Does the equilibrium condition prevail? How do you know?
iii. [2.5 pts] Roughly sketch *n* and *p* versus x.
iv. [2.5 pts] Sketch the electrostatic potential as a function of x.

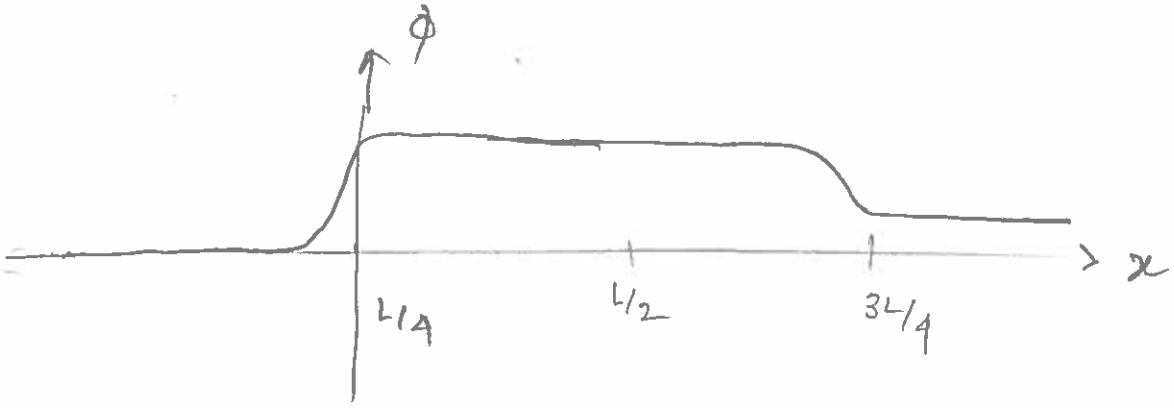
i. PNP

ii. yes because the Fermi level is flat.

iii.

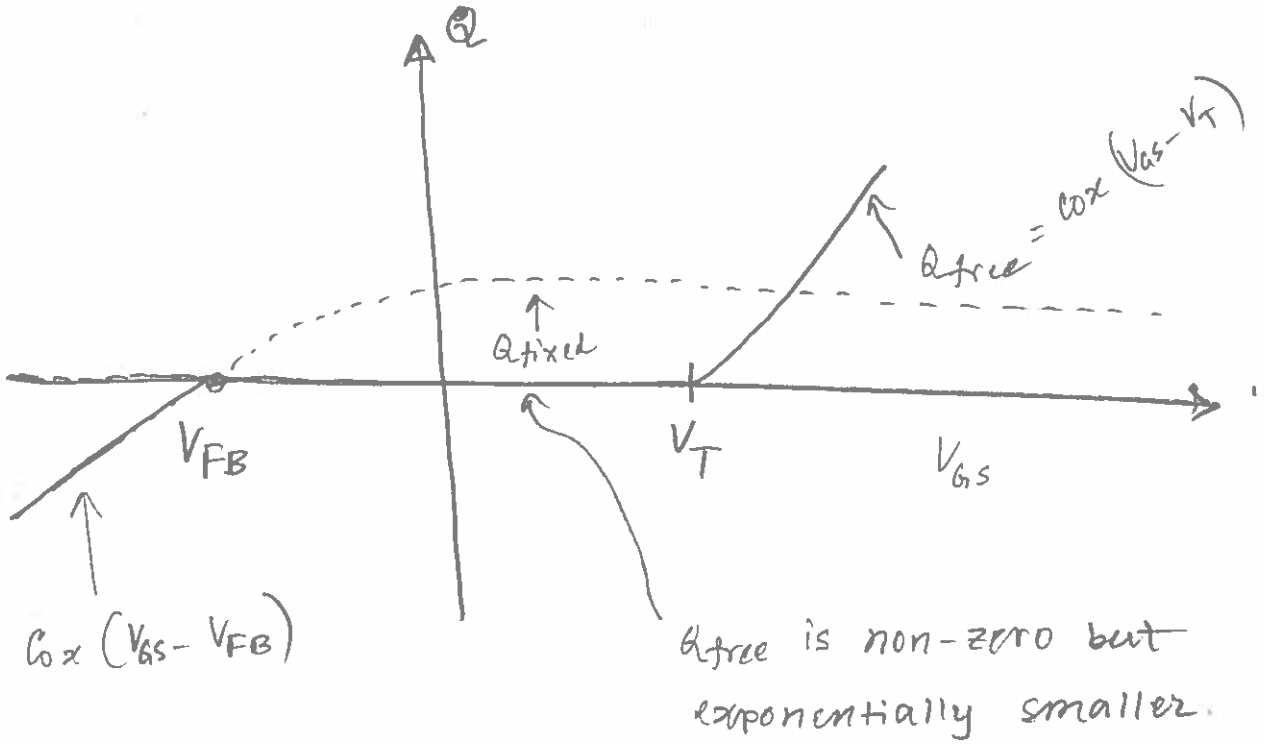


iv.



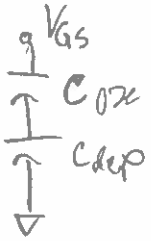
Prob 2 [20 pts]

(a) [8 pts] Qualitatively plot the free carrier density as a function of gate voltage in a MOS-capacitor with p-type body. On the same plot show the fixed carrier density as a function of gate voltage. Your plot should clearly show the flatband and threshold voltage points. Assume that the MOS capacitor has highly n^+ doped source /drain regions which are both grounded along with the body for this problem and the only voltage being applied is on the gate.



(b) [4 pts] If it is known that the depletion region width at Vgs=V_T is 500 nm and the body factor m is 1.3, what is the minimum capacitance? [V_T is the threshold voltage of the MOSFET]

Minimum capacitance occurs at $V_{GS} = V_T$ where the capacitive network of the depletion region is still valid



$$\therefore \frac{C}{min} = \frac{C_{dep\_min}\, C_{ox}}{C_{ox} + C_{dep\_min}}$$

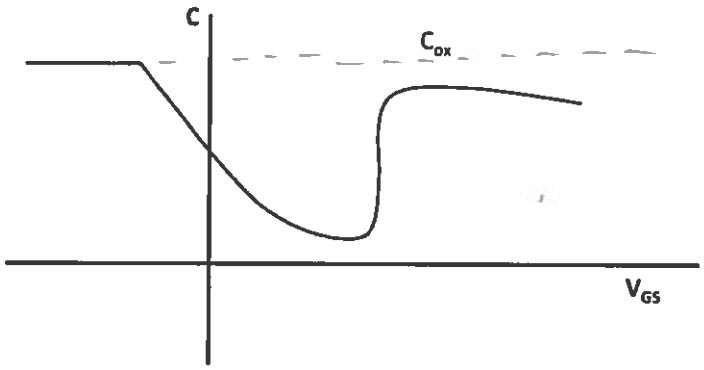
$$= \frac{C_{dep\_min}}{1 + \frac{C_{dep\_min}}{C_{ox}}} = \frac{C_{dep\_min}}{m}$$

$$\therefore C_{min} = \frac{\varepsilon_{si}}{m W_{T max}}$$

$$= \frac{11.9 \times 8.854 \times 10^{-14}}{1.3 \times 500 \times 10^{-7}}$$

$$\boxed{C_{min} = 1.5 \times 10^{-8} \text{ F/cm}^2}$$

(c) [4 pts] The C-V diagram of a MOS capacitor is shown in the following. Why is the capacitance in the inversion region different from $Cox=e_{ox}/t_{ox}$ where t_{ox} is the physical thickness of the insulator. How would a high-k-metal gate (HKMG) technology change it?



The capacitance in the inversion region is different because

(i) inversion charge is removed from the si/SiO_2 interface

(ii) if a poly-gate is used, then there is a poly depletion width.

HKMG will make C closer to Cox by removing the poly depletion region.

(d) [4 pts] What characteristic in the MOSFET shows the signature of velocity saturation. Can the carrier velocity increase even more after the velocity saturation has happened if the channel length is further reduced? Why /Why not?

$I_D - V_D$ characteristic shows linear spacing between traces for different V_g rather than quadratic, in the saturation region

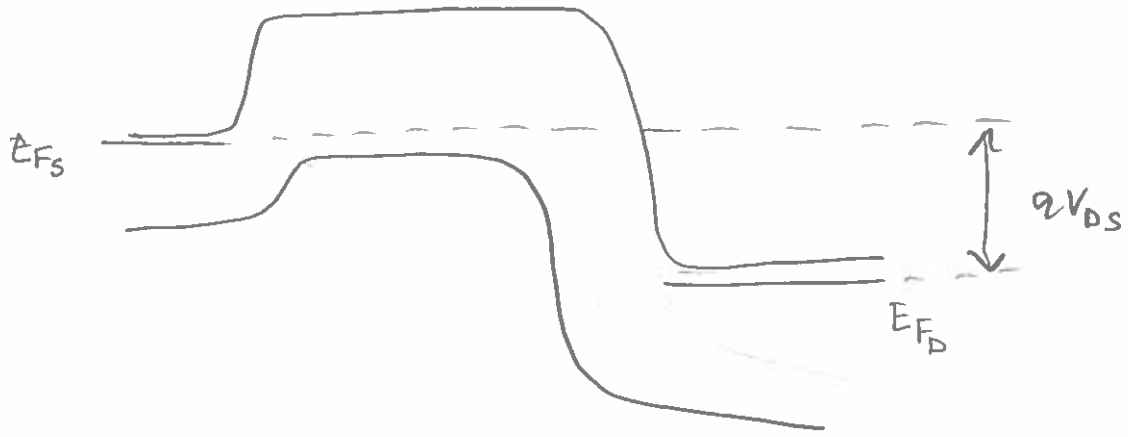
$I_{Dsat} \propto V_{GS}$

The velocity can still increase. This is because for a very small channel length carriers may not get enough time to scatter. Scattering is what otherwise determines saturation velocity at high electric fields.

Problem 3 [20 pts].

Problem 3a. Consider a Si MOSFET with p-type body is being operated at $V_{GS}<V_T$ (V_T is the threshold voltage). The drain voltage is set to a high value.

(i) [4 pts] Draw the band diagram at the Si/SiO_2 interface looking from source to drain.

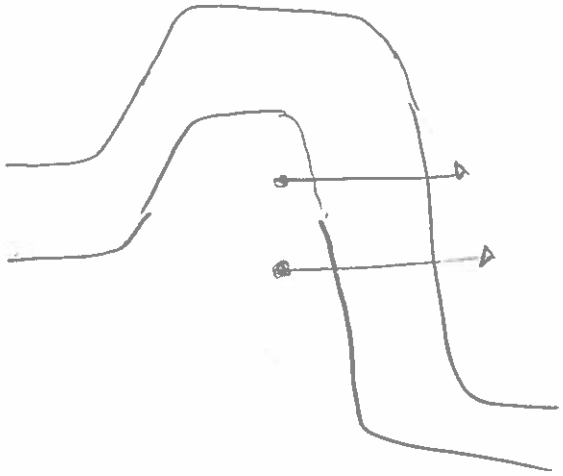


(ii) [4 pts] Briefly describe how current flows in this regime.

The current flow happens by injecting carriers from the source to the body akin to a p-n junction diode. Moreover, carriers are swept out at the drain side by creating a depletion region. This keeps a concentration gradient across the body leading to diffusion of carriers and current flow.

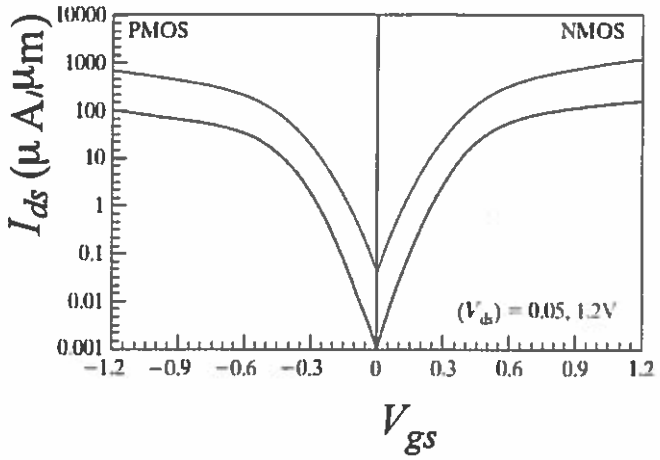
(iii) [4 pts] If the voltage is continuously reduced, how will the current change?

Initially the current will go down exponentially. However at some point carriers will start to tunnel from p- body to the drain, leading to an increase in current.



Problem 3(b) [8 pts]

Consider the following characteristic for a Si MOSFET where a change in the id-VG characteristic is seen as a function of drain voltage.



(i) [4 pts] What is this effect called? Briefly explain why this happens.

This effect is called DIBL (Drain induced barrier lowering) or V_T roll-off.

As the channel length is reduced so that the drain voltage depletion region reaches the source side p-n junction, increasing drain voltage can reduces the barrier height seen by the source electrons. As a result, current goes up.

(ii) [4 pts] Will this effect be better or worse for a material with larger permittivity than Si (11.9) such as InAs (12.3)?

$$W \propto \sqrt{\frac{2\varepsilon}{qN}}$$

so, for the same doping, larger ε leads to increase depletion width. This means that for the same channel length, drain side depletion region will reach the soure p-n junction at a smaller V_{DS}.

Therefore, the effect will become worse.