FINAL SOLUTION

Prob.	Score
1+2	/18
3	/12
4+5	/16
6	/10
7+8	/24
9	/20
10+11	/22
12+13	/22
14	/16
Total	/160

EECS140 Spring 2015 Final

Name Mr B+ student.

SID _____

1) [10] You need an amplifier with a gain of 10 at 10Mrad/s, and the gain must be accurate to 0.1%. You decide to use an op-amp in feedback. You may assume that the ratio of passives is perfect.
   a) What is the minimum low frequency gain of your op-amp?

   $f=0.1 \quad \frac{1}{Af} < 10^{-3} \quad A > \frac{1}{10^{-4}} = 10^4$

   b) What is the minimum unity gain frequency of your op-amp?

   $\omega_u > A\omega_p = 10^4 10^7 = 10^{11}$ rad/sec

   c) If your amplifier must drive a 1pF load capacitor, what is the minimum g_m required in the differential pair?

   $\omega_u \leq \frac{g_m}{C_L} \quad g_m > \omega_u C_L = 10^{11} 10^{-12} = 0.15$

   d) What is the minimum current consumption in the differential pair?

   $g_m = \frac{2I_D}{n V_T} \quad I_D > (40mV)(0.15) = 4mA$ → 8mA

   e) Explain why your answer to 1c is the same whether the op-amp is a two-stage or a single-stage.

   Single stage $\omega_u = \frac{g_m}{C_L}$

   Two stage in feedback assume PM > 45°, so $\omega_u = \frac{g_m}{C_L}$ $\omega_{p2} > \omega_u$, $\omega_{p2} = \frac{g_{m2}}{C_L}$

BAD +2 to everyone

2) [8] Assume that you are working with a single-sided supply of 5V in a technology with Vtn=|Vtp|=1V and you can choose from the following opamp topologies:
   (1) NMOS input folded cascode
   (2) PMOS input folded cascode
   (3) NMOS input 2 stage Miller compensated
   (4) PMOS input 2 stage Miller compensated
   (5) NMOS input folded cascode with output stage
   (6) PMOS input folded cascode with output stage

Which will work for each of the following applications (write all the numbers that will work for each)

   a) an opamp in unity-gain feedback with input from 2 to 5V and capacitive load.

   3 5

   b) a switched capacitor amplifier with a gain of +10 and input from 0 to 0.5V.

   6

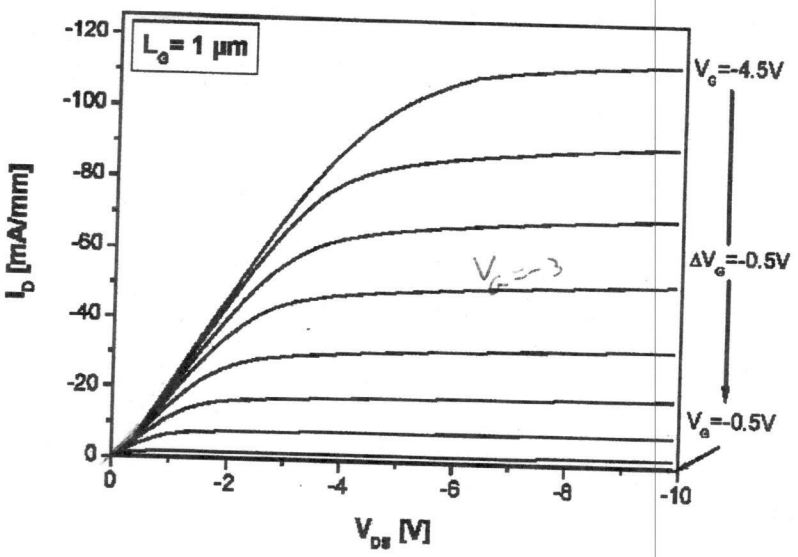
   c) an amplifier with a gain of 2 driving a 1kΩ resistive load and input from 0.5 to 1V

   4 6

   d) a unity-gain amplifier with input from 1.5 to 3.5V

   1 2 3 4 5 6

3) [12] The data in the figure below is taken from a **PMOS** transistor made out of diamond. The source is grounded, the drain voltage varies from 0 to -10V. The gate voltage varies from -0.5 to -4.5V in steps of -0.5V. Drain current is given in mA per millimeter of Width. Assume that you have a transistor that with W/L = 1000u/1u, so the vertical axis can be read as mA.



(from Kunze, et al., Carbon 37 (1999).)

2 a) estimate the threshold voltage, Vtp $\approx -0.5V$

2 b) estimate g_m when V_G=-3V and the device is in saturation

$\Delta I = 20mA$
$\Delta V = 0.5V$ $\quad g_m = 40mS$

2 c) estimate r_o when V_G=-3V and the device is in saturation

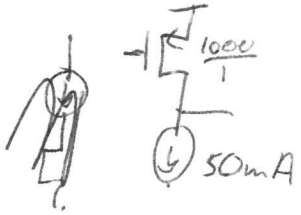
$\Delta I = 1mA$
$\Delta V = 5V$ $\quad R_o = \frac{\Delta V}{\Delta I} = \frac{5V}{1mA} = 5K$ ~1kΩ also okay

2 d) estimate R_{ON} when V_G=-4.5V and V_{DS}=0

$R_{ON} \approx \frac{1V}{20mA} = 50\Omega$

e) if this device is used as a PMOS common source amplifier with an ideal current source load at a gate bias of V_G=-3V,

4 (1) sketch the circuit, including the magnitude (in mA) of the current source
(2) roughly what gain will it have?



$A_V = -(40mS)(5K) = -200$

4) [10] Your colleague creates a new transistor with a drain current given by $I_d = a\, V_g\, V_d$ when the source is grounded. a has units of [A/V^2].

a) write a formula for g_m in terms of a, V_g, and V_d

2 aV_D

b) write a formula for r_o in terms of a, V_g, and V_d

2 $\frac{1}{aV_g}$

c) write a formula for the gain in terms of a, V_g, and V_d

2 $\frac{V_D}{V_G}$

d) for proper operation, you have to bias the gate and drain at values between 0.1V or 1V. Which values should you choose to maximize the gain?

4 $V_D = 1V$ $V_G = 0.1V$

5) [6] You are helping another colleague make measurements on an amplifier circuit in a box with three terminals labeled IN, OUT, and GND. You apply voltages from GND to IN and GND to OUT and measure the current as shown in the table below.

a) What is G_M for the amplifier?

2 $\frac{10mA}{1mV} = 10mS$

b) What is R_o for the amplifier?

2 $\frac{1mV}{1nA} = 1M\Omega$

c) If you disconnect the voltage source from OUT and apply 1.002V to IN, what voltage do you expect to see out OUT?

2 $3 - (0.002)(100) = 2.8V$

$3 - (0.002)(10{,}000) = -17V$

voltage on IN	voltage on OUT	current into IN	current into OUT
1V	3V	0	0
1.001V	3V	0	10uA
1V	3.001V	0	1nA

?? $3 - (0.002) * (1E-2)(1E9)$

$3 - 20 = -17V$?

6) [10] You have made a bandgap reference similar to the one in Lab 5. ***Carefully*** sketch the voltage across the diode, the voltage across resistor R_1, and the voltage at the drain of M1, all vs. temperature for T=-40 to +85C. "Carefully" means label each axis and draw clearly. Assume that the diode voltage is 0.6V at 25C, and ln(N)=1.

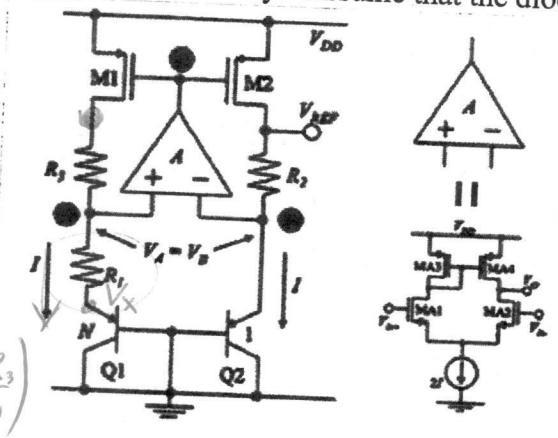


Fig. 6: A CMOS bandgap voltage reference using error-amplifier-based current mirror.

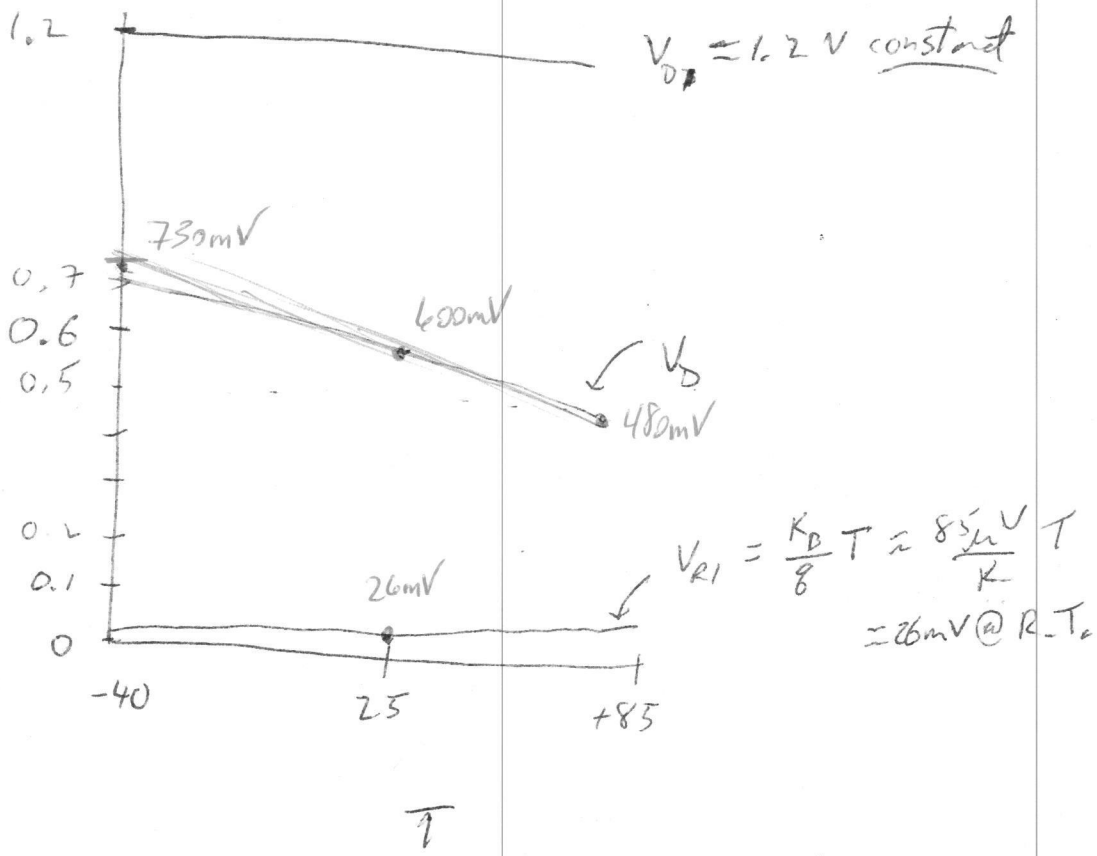
$V_{R3} = \frac{\Delta V_{BE}}{R_1} \cdot R_3$

$V_{DD} = V_X + \Delta V_{BE}\left(1 + \frac{R_3}{R_1}\right)$

slope of V_D : 3 pts

(V_{R_1}) slope of ΔV_{BE} : 3 pts

slope of V_{M1_D} : 4 pts

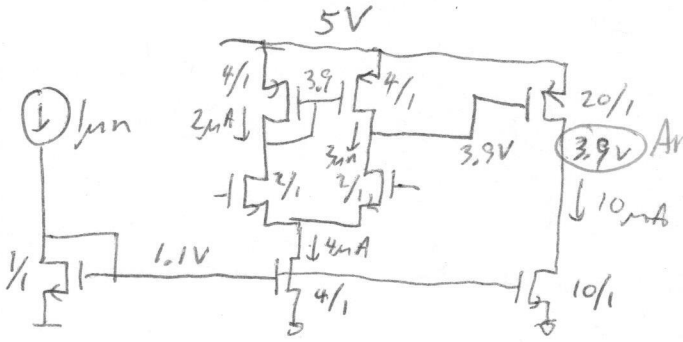


$V_{R_1} = \Delta V_{BE} = kT \ln(N)$ *

$\sim 26mV$ @ 25C

7) [16] Design an NMOS-input two-stage op-amp with the following specs:
- 2uA flowing in each input device and 10uA flowing in the output devices
- 100mV overdrive voltages
- 1um channel lengths
- V_{DD}=5V. $\mu_n C_{ox}$=200uA/V^2, $\mu_p C_{ox}$=100uA/V^2, $|V_{tp}|=V_{tn}$=1V, λ=1/(10V)

You may use a single 1uA ideal current source or sink. Draw a clean, clear schematic, label your devices, label node voltages and branch currents.



Any answer [0.5] okay

$\frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{OV})^2 = 1\mu A$ $\left(\frac{W}{L}\right)$

$\frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{OV})^2 = 0.5\mu A$ $\left(\frac{W}{L}\right)$

$g_{m1} = \frac{2I_D}{V_{OV}} = \frac{4\mu A}{100mV} = 40\mu S$

$G_{m2} = \frac{20\mu A}{100mV} = 200\mu S$

$A_{v1} = -100$

$R_{o1} = \frac{1}{2}\frac{10V}{2\mu A} = 2.5M\Omega$

$A_{v2} = -100$

$R_{o2} = \frac{1}{2}\frac{10V}{10\mu A} = 500k\Omega$

8) [8] For the previous problem,
a) what is the input common mode range [1.2, 4.9]

b) output swing [0.1, 4.9]

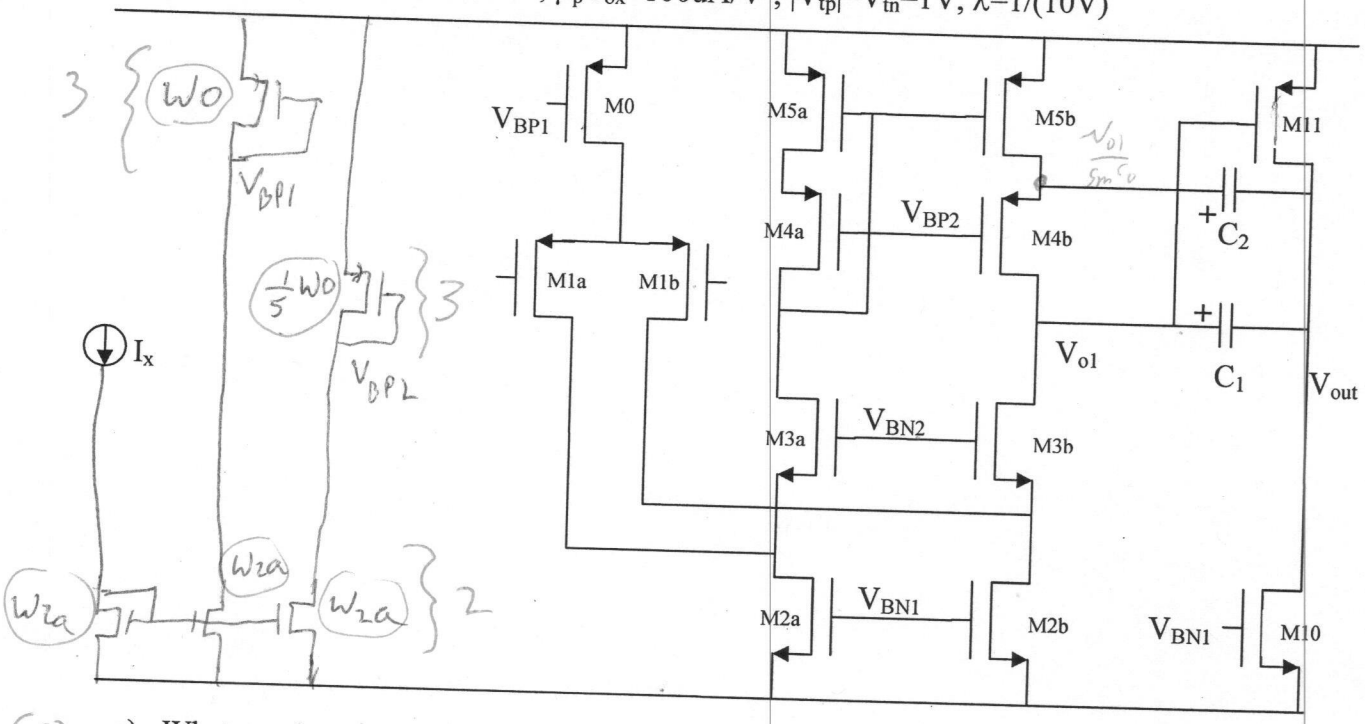
c) low frequency gain 10,000

d) output pole with a 10fF load capacitor?

$\frac{1}{(500K)(10fF)} = \frac{1}{5n} = 0.2G\frac{rad}{sec}$

9) [20] For the amplifier below, assume that you have designed the circuit such that

- $I_{D0}=I_{D2a}=I_{D10}$
- 100mV overdrive voltages, 1um channel lengths
- $V_{OUT} = V_{DD}/2$
- V_{DD}=5V. $\mu_n C_{ox}$=200uA/V^2, $\mu_p C_{ox}$=100uA/V^2, $|V_{tp}|=V_{tn}$=1V, λ=1/(10V)



[5] a) What are the widths of M1a, M4a, M5a and M11 in terms of W_0?

W1a= 1/2 W0	W4a= 1/2 W0	W5a= 1/2 W0	W11= W0

b) What are the widths of M3a and M10 in terms of W_{2a}?

[2]

W3a= 1/2 W2A	W10= W2A

[1] c) What is the bias voltage on V_{o1} with V_{id}=0? 3.9V

[2] d) What is the input common mode range? $[V_{BN2} - 0.1V - |V_{tp}|, 3.8V]$ -0.9 is -1

[2] e) What is the output swing? [0.1, 4.9] V -1 for [0,5]

[8] f) Using the ideal current source with current $I_x=I_{D0}$, design the bias circuitry just for the PMOS gates, V_{BP1} and V_{BP2}. Label device sizes relative to W0 and W2a.

10) [12] In the previous problem, C_1 connects the *drain* of M4b to the output. C_2 connects the *source* of M4b to the output. Assume that the gain of the second stage is A_{v2}. When a differential input causes a small signal change v_{o1} on the folded cascode

a) What is the voltage across C1? $(1-A_{v2})\,v_{o1}$ (1)

b) What is the voltage across C2? $-A_{v2}\,v_{o1}$ (1)

c) What is the current in C1? $(1-A_{v2})\,v_{o1}\,s\,C_1$ (2)

d) What is the current in C2? $-A_{v2}\,v_{o1}\,s\,C_2$ (2)

e) Is there significant feedforward current in C1 causing a RHP zero? yes (1)

f) Is there significant feedforward current in C2 causing a RHP zero? NO (1)

g) What is the effective capacitance seen at V_{o1} due to C1, if any? $(1-A_{v2})\,C_1$ (2)

h) What is the effective capacitance seen at V_{o1} due to C2, if any? $-A_{v2}\,C_2$ (2)

11) [10] Consider a simple two-transistor amplifier: an NMOS-input common source amplifier with PMOS load. Assume that the PMOS device has an overdrive voltage twice the NMOS overdrive voltage.

a) What is the PMOS transconductance, g_{mp}, in terms of the NMOS transconductance g_{mn}? $g_{mp} = \frac{2I_d}{V_{ovp}} = \frac{1}{2} g_{mn}$ (2)

b) What is the gain from the PMOS device to the output, A_{vp}, in terms of the NMOS gain to the output, A_{vn}? $A_{vp} = \frac{1}{2} A_{vn}$ (2)

c) What is the thermal noise voltage in the PMOS device, v_{np}, in terms of the thermal noise voltage in the NMOS device, v_{nn}? $\overline{v}_{n,p}^2 = 4kT\frac{1}{g_m}\,0f = \frac{3}{2}\overline{v}_{nn}^2$ $\qquad \overline{v}_{n,p} = \sqrt{2}\,\overline{v}_{n,n}$ (2)

d) What is the total output noise power, $(v_{noise,out})^2$? $\overline{v}_{n,n}^2 A_{vn}^2 + \overline{v}_{n,p}^2 A_{vp}^2 = \overline{v}_{n,n}^2 A_{vn}^2\left(1+2\left(\frac{1}{2}\right)^2\right) = \frac{3}{2}\overline{v}_{n,n}^2 A_{vn}^2$ (2)

e) What is the total equivalent input noise power, $(v_{noise,inputEQ})^2$ in terms of the NMOS noise voltage? $\left(\sqrt{\frac{3}{2}}\,\overline{v}_{n,n}\right)^2$ (2)

12) [12] A circuit similar to the PGA in your final project has a 10fF capacitor pulled to ground by a 1u/0.1u transistor. With Cox=5fF/um2, Col'=0.5fF/um, Vtn=0.2V, and with Vdda=1.2V, estimate the effect of charge injection on the capacitor voltage after the falling edge of the clock assuming

$C_{gs} = 0.5fF$ $C_{ol} = 0.5fF$

a) a fast-clocked circuit

$\Delta V = \frac{(C_{gs}+C_{ol})V_{DDA}}{C} = \frac{1fF}{10fF}\,1.2V = 0.12V$

ϕ 1 2 C

$\Delta V = \frac{C_{ox}WL(V_{DD}-V_t)}{2C}$

$= 25mV$

b) a slow-clocked circuit

$\Delta V = \frac{C_{ol}V_{tn}}{C} = \frac{(0.5fF)(0.2V)}{10fF} = 10mV$

If $\mu_n C_{ox}$=200uA/V^2

c) estimate the time necessary for the voltage to fall from 1mV to 0.05mV. Clearly show your reasoning and calculations!

95% fall $\Rightarrow$ $3\tau = 15ps$

$\tau = R_{ON}C = (500)(10^{-14}) = 5\times10^{-12}s$

$R_{ON} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)} = \frac{1}{200\frac{\mu A}{V^2}(10)(1V)^2} = \frac{1}{2\,mA/V} = 500\Omega$

d) If you are not happy with the time that it takes for the voltage to fall from 1mV to 0.05mV, what are two things that you can change in the design that will cause the voltage to fall faster, and what impact (bigger, smaller, or no change) do they have on your answers to parts a and b above?

make W wider } both make ΔV worse

make C smaller }

make L shorter - makes 12a better, 12b the same.

+1 for 2 suggestions.

+2 for impacts on (a) and (b)

13) [10] An op-amp with open-loop differential input capacitance C, output resistance R, and voltage gain A is put into feedback with a closed-loop voltage gain A_{CL}. If you measure the closed-loop input capacitance and output resistance, what will they be?

$f = \frac{1}{A_{CL}}$ +3 for this realization.

$C_{in} = \frac{C}{1+Af} = \frac{C}{1+A/A_{CL}}$

C_{in} goes down by Af or 1+Af

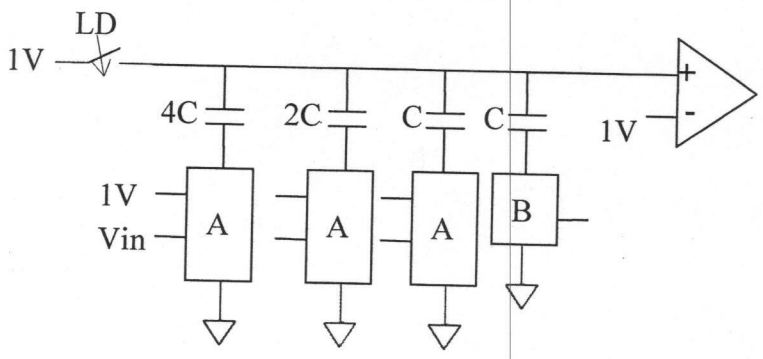
+1 for this +1

$R_{out} = \frac{R}{1+Af} = \frac{R}{1+A/A_{CL}}$

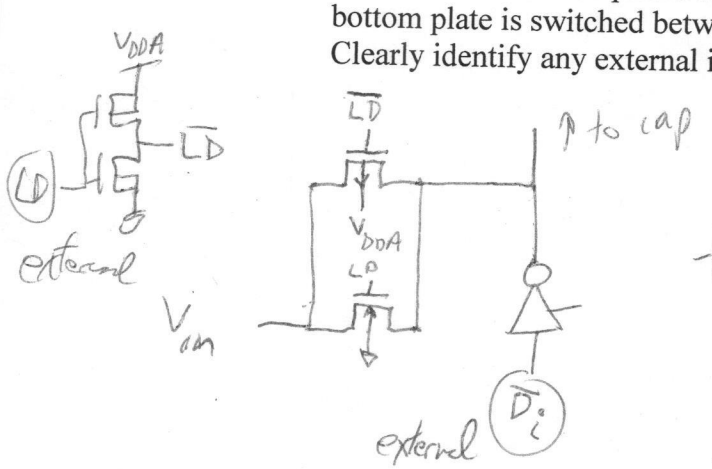
Rout goes down by Af or 1+Af.

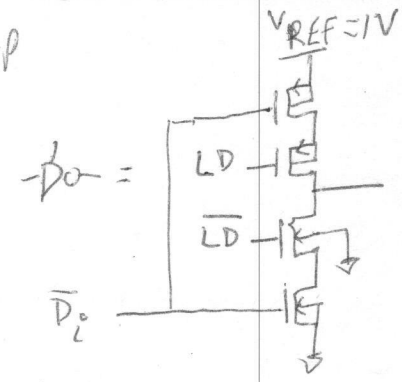
+1 for this +1. sorry I had to be consistent :-

14) [16] Many student projects used a topology like the following ADC in their final projects. An external digital SAR circuit takes a clock and the comparator output and generates the LD and Di signals.



[8] a) design the circuitry that goes inside of the boxes labeled A, assuming that Vin is loaded on the bottom plates of the capacitors during the LD phase, and then the bottom plate is switched between 1V and ground in subsequent clock cycles. Clearly identify any external inputs to the box which are currently not shown.





[2] Drive Vin, 1, 0
[2] with LD D_i $\overline{D_i}$ ideal switches
[2] good switches
[2] inverters etc

[8] b) Assuming the SAR drives the signals to the boxes properly, sketch the waveforms on LD, the digital control bits D2, D1, and D0, and V+ when the input Vin = 0.6V