Problem 2: Device Analysis

Consider the device configuration of FIG. 2. M1 is

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EECS 141: FALL 00 —MIDTERM 1

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:

$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last SOLUTION First

GRAD/UNDERGRAD	

Problem 1: 8.5

Problem 2: 10.0

Problem 3: 7.5

Total	26

PROBLEM 1: Transient Response

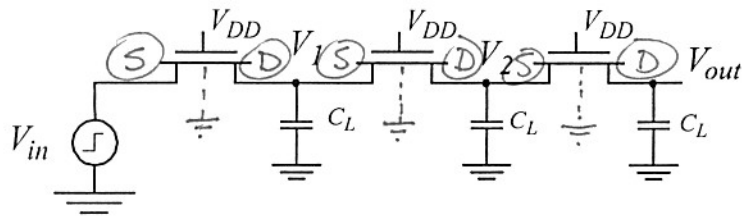


FIG. 1 Digital circuit

Consider the circuit of FIG. 1. All the transistors are originally minimum-size devices. Use the transistor parameters indicated on the first page of the midterm. V_{DD} = **2.5 V**. C_L = 30 fF. Leakage effects should not be considered in this question.

a. Assume that the initial voltage on V_{out} = 0. A step from 0 to V_{DD} is applied at the input. Determine the final voltage at V_{out}.

(1) $V_{OUT} = V_2 = V_1 = V_{GS} - V_T \Rightarrow V_T = V_{DD} - V_1$

(1) $V_T = V_{Tn} + \gamma\left[\sqrt{-2\phi_F + V_{SB}} - \sqrt{-2\phi_F}\right]$; $V_{SB} = V_1$

body effect

$2.5 - V_1 = 0.4 + 0.4\left[\sqrt{0.6+V_1} - \sqrt{0.6}\right]$

$(2.41 - V_1)^2 = (0.4\sqrt{0.6+V_1})^2$

$2.41^2 - 4.82V_1 + V_1 = (0.16)(0.6 + V_1)$

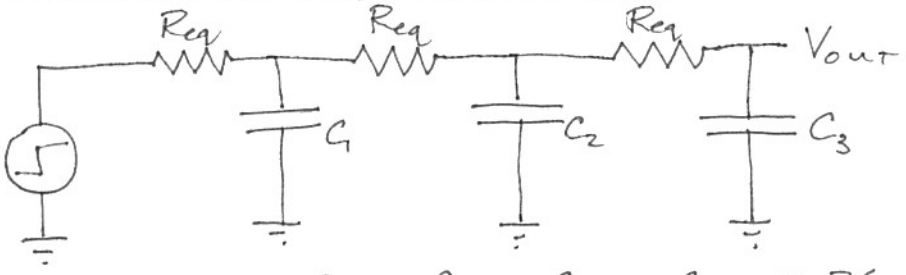
$V_1^2 - 4.916V_1 + 5.664 = 0$

could have iterated (trial + error) as well

(0.5) **V_{out} (final) =** 1.843 V

b. Assume the following parameters for the minimum size transistors: R_{eq} = 15 kΩ, C_{gs} = C_{gd} = C_{gb} = 1fF. C_{sb} = C_{db} = 2 fF. To determine the propagation delay of the circuit, we will use the equivalent resistor-capacitor diagram. Draw the equivalent circuit including all **relevant** resistors and capacitors and their values.

(2)



$C_1 = C_{GD} + C_{DB} + C_L + C_{GS} + C_{SB}$ = 36 fF

$C_2 = C_{GD} + C_{DB} + C_L + C_{GS} + C_{SB}$ = 36 fF

$C_3 = C_{GD} + C_{DB} + C_L$ = 33 fF

c. Determine the **propagation delay** between input and output for a step at the input from 0 to Vdd.

(1.5)
$$\tau = R_{eq}C_1 + 2R_{eq}C_2 + 3R_{eq}C_3$$
$$= (15k)(36f) + (30k)(36f) + (45k)(33f)$$
$$= 3.105 \text{ ns}$$

(0.5)
$$t_{pd} = 0.69\,\tau = 2.142 \text{ ns}$$

t_p(for *Vin* going from *0* → Vdd)= 2.142 ns

d. Assuming that the transistor capacitors and conductance increase linearly with the width of the transistor. Determine the size *S* of the transistors that reduces the propagation delay by a factor of 2. All three transistors are to be scaled by the same factor..

(1.5)
$$\tau_S = \left(\frac{R_{eq}}{S}\right)(6f \cdot S + C_L) + \left(\frac{2R_{eq}}{S}\right)(6f \cdot S + C_L) + \left(\frac{3R_{eq}}{S}\right)(3f \cdot S + C_L)$$

$$\frac{\tau}{2} = \tau_S$$

$$\frac{1}{2}[36 + 72 + 99] = \left(\frac{1}{S}\right)[65 + 30 + 125 + 60 + 95 + 90]$$

$$76.5S = 180$$

$$S = 2.353$$

(0.5)

$S = (W/L) / (W/L)_{orig}$ = 2.353

Problem 2: Device Analysis

Consider the device configuration of FIG. 2. M1 is a minimum size transistor (assume W/L = 1). Assume the transistor parameters given on page 1 of the midterm, but assume that $\gamma = 0$ (no body-effect). Assume a short-channel transistor modeled by the unified model..

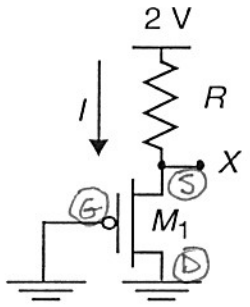


FIG. 2 CMOS inverter with resistive load

a. Write down the equations (and only those) that you need to determine the voltage at node *X*. Do NOT plug in any values yet. BE COMPLETE and CONSIDER ALL POSSIBLE SOLUTIONS. Determine for each solution when it is valid.

Notice that $V_{GS} = V_{DS}$ $\therefore$ M_1 is always either in saturation or vel. saturation

$$I_D = \frac{2 - V_X}{R}$$

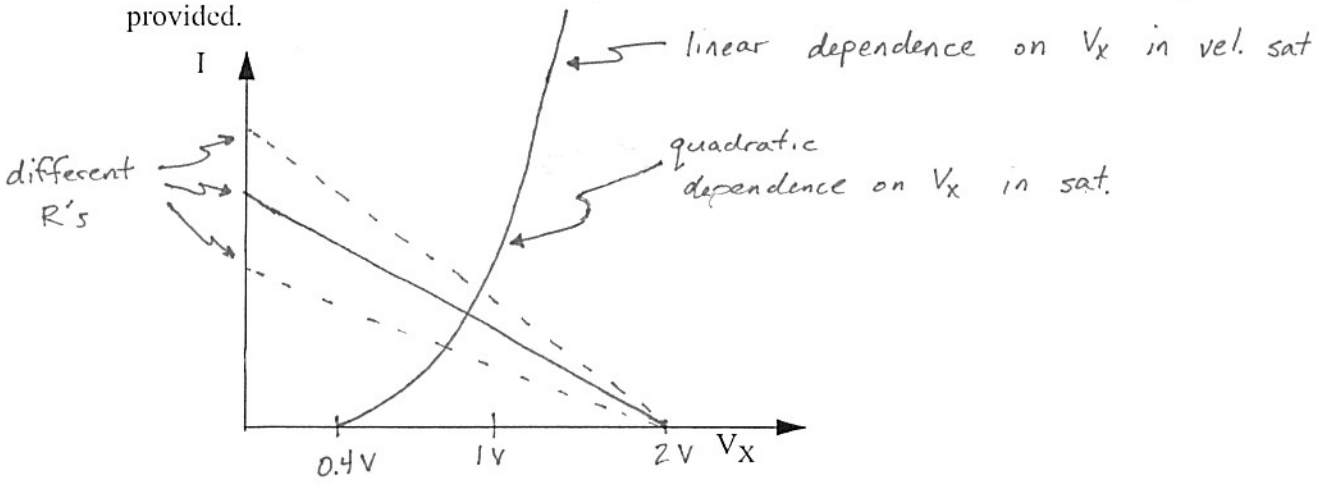
If M_1 in saturation $(V_X < 1V)$, $V_{MIN} = |V_{GS}| - |V_T| = 0.8 - 0.4 = 0.4$

$$I_D = \frac{1}{2} k_p' \left(\frac{W}{L}\right)\left[(|V_X| - |V_{T_p}|)^2\right]$$

If M_1 in vel. saturation

$$I_D = k_p'\left(\frac{W}{L}\right)\left[(|V_X| - |V_{T_p}|)|V_{DSAT_p}| - \frac{|V_{DSAT_p}|^2}{2}\right]$$

b. We would like to place V_X at 0.8 V. Determine which of the above soltuions is valid. Draw the (approximative) load lines for both MOS transistor and resistor on the diagram provided.



c. Determine the value of the resistance required to place X at 0.8V.

If $V_X = 0.8V$, M_1 in saturation since $|V_{DS}| < |V_{DSAT_p}|$

$$\frac{2-0.8}{R} = \left(\frac{1}{2}\right)(30\cdot 10^{-6})(0.8-0.4)^2$$

$$R = \frac{1.2\ V}{2.4\ \mu A} = 500\ k\Omega$$

R= 500 kΩ

d. Assume now that the λ-factor of the PMOS is different from 0, in contrast to what was assumed so far. Determine qualitatively if the voltage at node X will go down, or up, or remain unchanged. Explain your answer.

- ☐ Up
- ☑ Down
- ☐ Unchanged

if $\lambda_p \neq 0$, then I increases, drawing more current through R

→ IR drop across R is larger

→ therefore V_X must decrease

PROBLEM 3: Technology Scaling

Consider a CMOS inverter followed by a wire on length L. Assume that in the reference design, inverter and wire contribute equally to the total propagation delay t_{pref}. You may assume that the transistors are velocity-saturated. The wire is scaled in line with the **ideal wire scaling model**. Assume initially that the wire is **a local wire**.

a. Determine the new (total) propagation delay as a a function of t_{pref}, assuming that technology and supply voltage scale with a factor 2. Consider only first-order effects.

Delay of buffer scales as $1/S$

Delay of local wires scales as 1

$$t_p = \frac{t_{p\,buffer}}{2} + t_{pwire} = \frac{t_{pref}}{4} + \frac{t_{pref}}{2} = \frac{3}{4} t_{pref}$$

(1) $t_p = 3/4\ t_{pref}$

b. Perform the same analysis, assuming now that the wire scales a **global wire**, and the wire length scales inversely proportional to the technology.

Delay of global wire scales as S^4

$$t_p = \frac{t_{pref}}{4} + \frac{t_{pref}}{2} \cdot 16 = \frac{33}{4} t_{pref}$$

(1) $t_p = 33/4\ t_{pref}$

c. Repeat b, but assume now that the wire is scaled along the constant resistance model. You may ignore the effect of the fringing capacitance.

Delay of global wire (constant resistance) scales as S^3

$$t_p = \frac{t_{pref}}{4} + \frac{t_{pref}}{2} \cdot 8 = \frac{17}{4} t_{pref}$$

(1) $t_p = 17/4\ t_{pref}$

d. Repeat b, but assume that the new technology uses a better wiring material that reduces the resistivity by half, and a dielectric with a 25% smaller permittivity.

$$t_p = \frac{t_{pref}}{4} + \frac{t_{pref}}{2} \cdot 16 \times \frac{1}{2} \times \frac{3}{4}$$

(resistivity) (dielectric)

(1) $t_p = 13/4\ t_{pref}$

e. Discuss the energy dissipation of a. as a function of the energy dissipation of the original design E_{ref}.

$E_{buffer} \sim CV^2$ $\quad C \to 1/5$

$E_{wire} \sim CV^2$ $\quad V \to 1/5$

So

E_{buffer} scales as $1/5^3$

E_{wire} scales as $1/5^3$

$$E = \frac{E_{ref}}{2} \cdot \left(\frac{1}{8}\right) + \frac{E_{ref}}{2} \cdot \frac{1}{8}$$

(1) $E = 1/8\ E_{ref}$

f. Determine for each of the statements below if it is true, false, or undefined, and explain in one line your answer.

(0.5) - When driving a small fan-out, increasing the driver transistor sizes raises the short-circuit power dissipation. (T) - F - U Overdriving the output causes the output fall time to be much smaller than the input rise time, increasing S.C. power

(0.5) - Reducing the supply voltage, while keeping the threshold voltage constant decreases the short-circuit power dissipation. (T) - F - U Less time when both transistors are on

(0.5) - Moving to Copper wires on a chip will enable us to build faster adders. T - (F) - U
RC delay is not an issue for short wires

(0.5) - Making a wire wider helps to reduce its RC delay. T - F - (U)
Only when fringing is an issue, but making a wide wire wider won't help

(0.5) - Going to dielectrics with a lower permittivity will make RC wire delay more important.
T - (F) - U
RC scales down in the same way as C → impact remains the same.