EECS 141: FALL 00 — MIDTERM 2

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:

$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	
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GRAD/UNDERGRAD	

Problem 1:

Problem 2:

Problem 3:

Total	

PROBLEM 1: Inductance
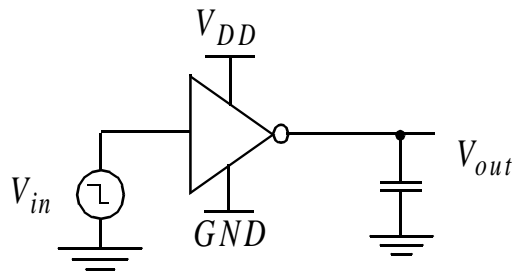
Consider the simple circuit of FIG. 1, where the inverter is implemented using complimentary CMOS. Assume that the transistors in the inverter can be modeled as constant linear resistors (when on). $V_{DD} = 2.5$ V. $C_L = 25$ pF. .

V_{DD}

V_{in}

GND

V_{out}

FIG. 1 Large Capacitance Driver

a. Assuming a 1->0 transition at the input, determine the **transistor resistances** that will result in a **0 to 90%** transition on the output of 5 nsec..

$\mathbf{R_{NMOS}} =$
$\mathbf{R_{PMOS}} =$

b. Draw the current drawn from the supply as a function of time during this low-to-high transition, and derive the appropriate equations that describe that behavior. Assume that the input signal has a very steep slope, and that the transistors switch instantaneously.

i_{VDD}

t

c. The supply rails of the driver (V_{DD} and GND) are connected to an **external off-chip supply** with a value of 2.5 V through bonding pads and wires with a total inductance of 7.5 nH. Draw the V_{DD} and GND signals as a function of time f**or the transition described above**, and annotate some meaningful values. You may assume that the introduced inductances do NOT impact the results of part b.

V_{DD}

t

GND

t
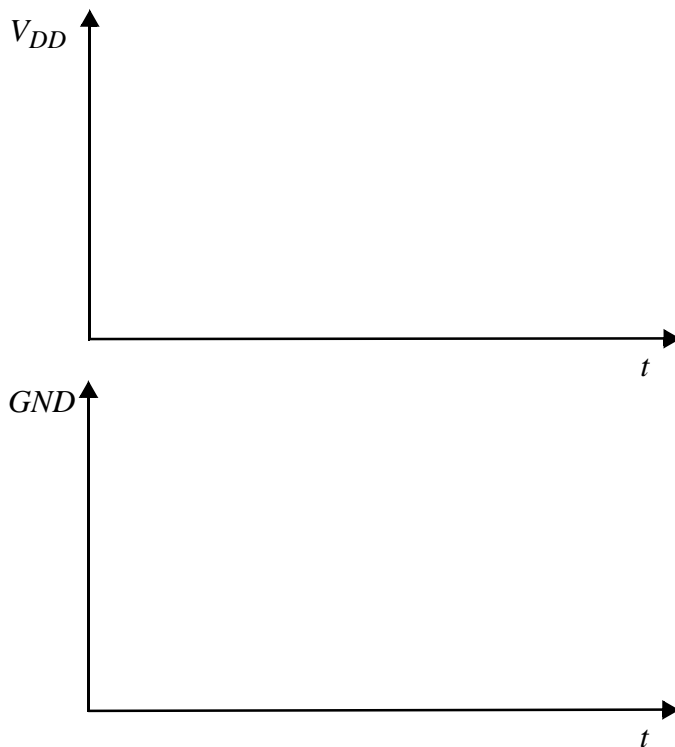
d. Faced with the emerging problem, rank-order the following remedies in order of potential effectiveness. 1 being the most effective, 4 the least

- Introduce a capacitance of 25 pF between V_{DD} and GND. ☐

- Increase the 0-90% rise/fall times at the output with a factor of 2 by reducing the transistor sizes. ☐

- Slow down the input signal to a fall time of 1 nsec. ☐

- Use copper instead of aluminum for the supply distribution network. ☐

Problem 2: Logic and Energy

Jari Tukkola, a cellular phone designer at Nokia, has come up with a bus-driving approach that he believes is going to both decrease energy consumption and increase performance. To deliver the high performance, he has started from a dynamic bus approach as shown in FIG. 2 for bit i. V_{DD} is set at 2.5 V.
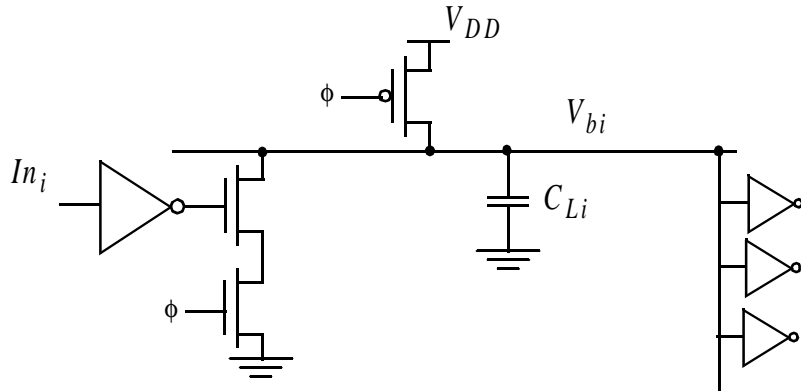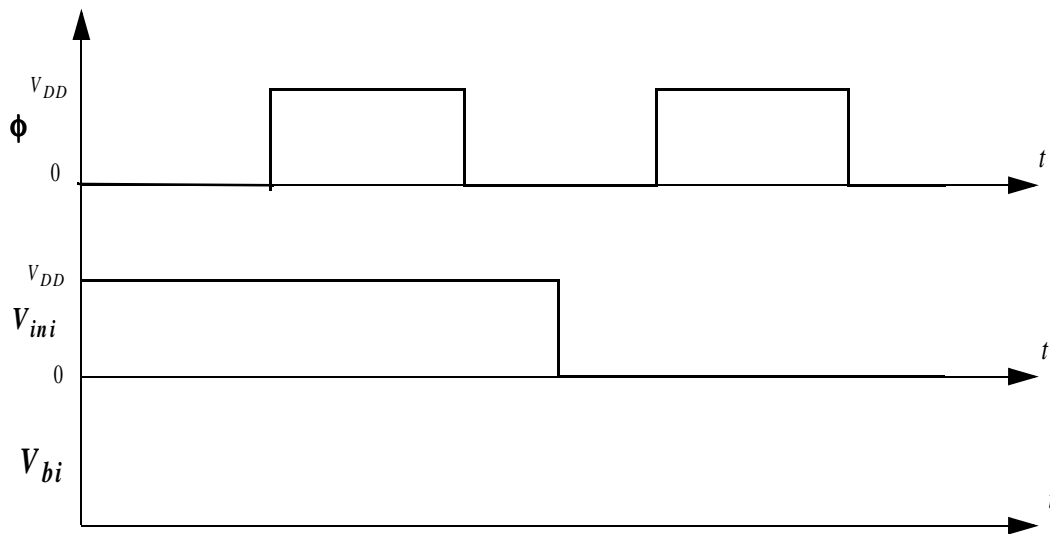

FIG. 2 Dynamic bus architecture (bit i)

a. Draw a timing diagram explaining the operation of the circuit (for the clock and input signals shown below).


b. The switching threshold of the bus fanout inverters INV has been optimized for optimal performance. Explain what Jari did to achieve this, and why.

c. For a bus width of $N=4$, determine the average energy dissipated per clock cycle for the whole bus, assuming that each input bit has a 50% chance of being a zero or a one. You may assume that the capacitive load of the bus wire $C_{Li} = 10$ pF dominates all other capacitances (including the clock capacitance, and the driver inverter).

$\boxed{\mathbf{E_{ave}=}}$

d. Jari believes that he could reduce the average energy dissipation of the bus if he would modify the circuit along the lines of FIG. 3, which replaces the driving inverter by a NEXOR. The logic block F outputs a "1" if the number of "0" bits in the input word is larger than the number of "1" bits. For instance, $F = 1$, if In = 0010; $F = 0$, if $In = 0011$ or $In = 1110$. Explain why this idea of Jari might not be a bad one after all.

FIG. 3 Modified dynamic bus architecture (bit i)
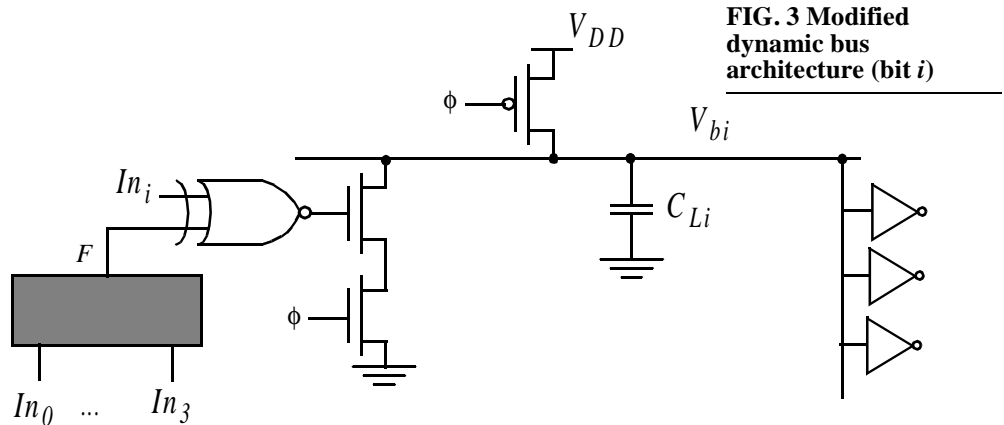
e. Design the gate that implements the logic block *F*. Derive first the required logic function, and consequently implement the gate in static complimentary CMOS. Make sure to size the transistors appropriately (this is, take into account the 3 times lower driving capability of the PMOS devices compared to NMOS, and assume that the gate has to have a driving capability equal to a minimum-sized NMOS inverter).

F=

e. Still assuming that each input bit has a 50% chance of being either a zero or a one, determine again the average energy dissipated per clock cycle. **(WARNING - THIS MIGHT TAKE TIME TO FIGURE OUT. RESERVE THIS FOR DESSERT)**.

E$_{ave}$=

PROBLEM 3: Dynamic Logic

Consider a conventional 4-stage Domino logic circuit as shown in Figure 6 in which all precharge and evaluate devices are clocked using a common clock ϕ. For this entire problem, assume that the pulldown network is simply a single NMOS device (i.e., each Domino stage consists of a dynamic inverter followed by a static inverter). Assume that each gate has a propagation delay of $T/2$ (with T a time unit). Hence, the precharge time of the dynamic gate is $T/2$, the evaluate time of the dynamic gate is $T/2$ and the inverter low-to-high and high-to-low transitions are each $T/2$. Assume that the transitions are ideal (zero rise/fall times).
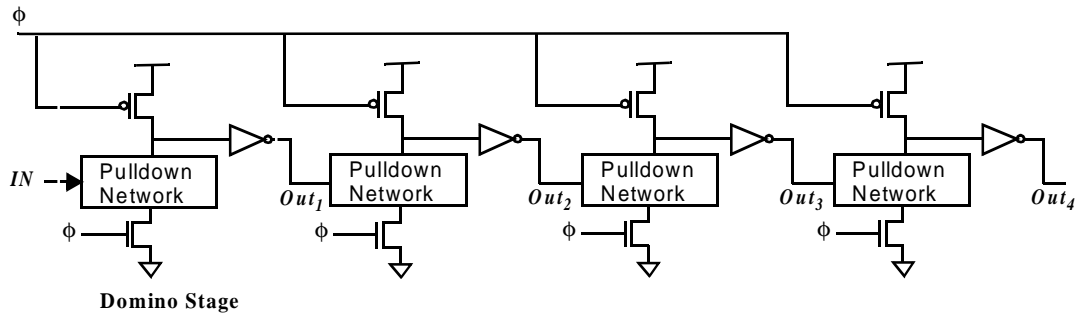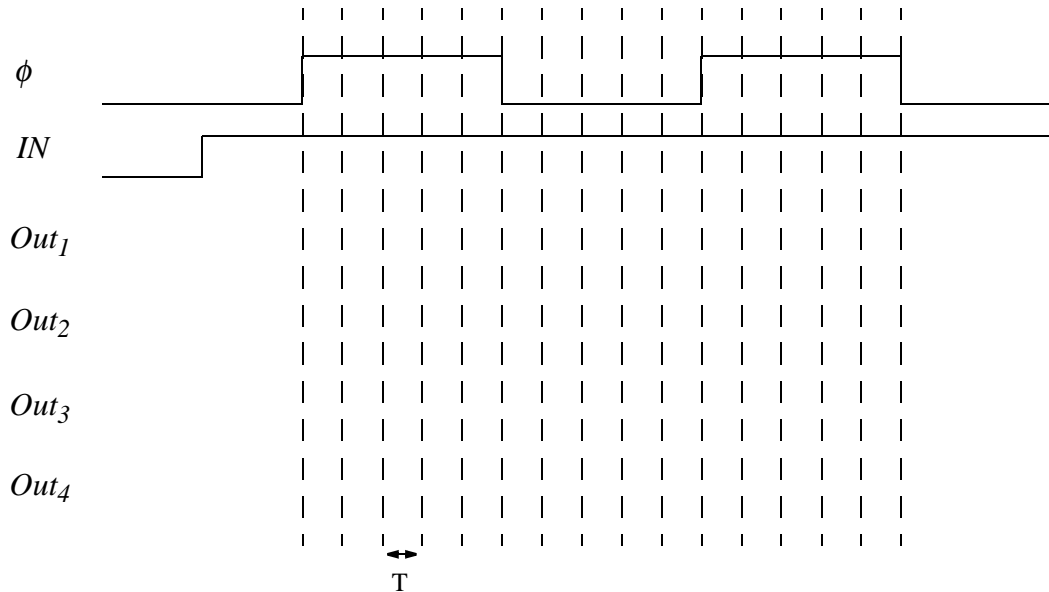

FIG. 4 Conventional Domino Dynamic Logic. Assume the pulldown network is a single NMOS device (i.e., each Domino stage consists of a dynamic inverter followed by a static inverter)

(a) Complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4.

Now consider the following variation of the circuit where the evaluate switch of the later stages have been removed.
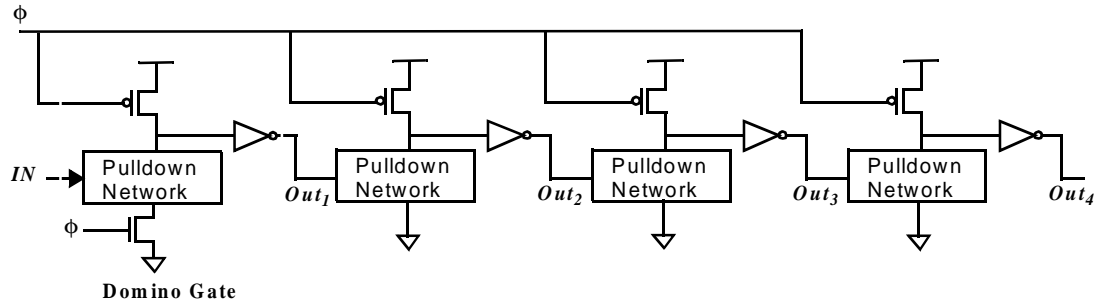

FIG. 5 Conventional Domino Dynamic Logic with the evaluate switches removed in the later stages.

(b) Assume that the clock ϕ is initially in the precharge state (ϕ=0 with all nodes settled to the correct precharge states), and the block enters the **evaluate** period (ϕ=1). Does the removal of the evaluate switches help or hurt the evaluation. Explain.

(c)Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the **precharge** state (ϕ = 0). Does the removal of the evaluate switches help or hurt the precharge. Explain.