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6:30-8:00pm

EECS 141: FALL 2001—MIDTERM 2

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):
NMOS:
$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$
PMOS:
$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME		
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GRAD/UNDERGRAD	

Problem 1: _____/ 8

Problem 2: _____/16

Problem 3: _____/12

Problem 4: _____/8

Problem 5: _____/10

Total: _____/54

PROBLEM 1. Logic Styles (8pts)

In this problem, for single-ended logic styles, assume that only true inputs are available, and for differential logic styles you can use both true and complementary inputs. Draw implementation of a two-input XOR gate in:

a) Standard complementary CMOS.

b) Domino logic.

c) Dual-rail domino.

d) Complementary pass-transistor logic (NMOS-only differential logic style)

PROBLEM 2. Logical effort. (16pts)

Consider two implementations of an 8-input AND gate:

- Design A consists of two 4-input domino AND gates, followed by a 2-input domino AND. Inverters in domino stages are high-skewed, with PMOS transistors being 4 times wider than NMOS.
- Design B consists of a two dynamic 4-input NAND gates, followed by a 2-input high-skewed static NOR (such that PMOS transistors are two times wider than NMOS).

You cannot eliminate the foot switch. Assume that the diffusion capacitance at the output node dominates the parasitic gate delay.

Your task is to compare the speed of these two designs. Please show your work and explain your reasons.

a)   (8pts) Which design is faster if the output capacitance is equal to the input capacitance?

b)   (8pts) Which design is faster if the output capacitance is 16 times larger then the input capacitance?

Based on this result, can you draw a conclusion about when you would include logic into a static gate that follows a dynamic gate?

PROBLEM 3: Arithmetic Circuits (12pts)
    You are asked to implement a partial product summation tree for a multiplier in two
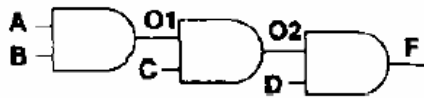   different logic styles.
    a) (8pts) Draw an implementation of a one-bit carry-save adder in single-rail domino
       logic and in transmission-gate logic.

    b) (4pts) Give two reasons why you might not want to use a domino implementation
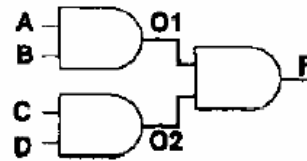   of a carry-save adder in a multiplier tree.

1.

2.

PROBLEM 4. Power dissipation (8 pts).
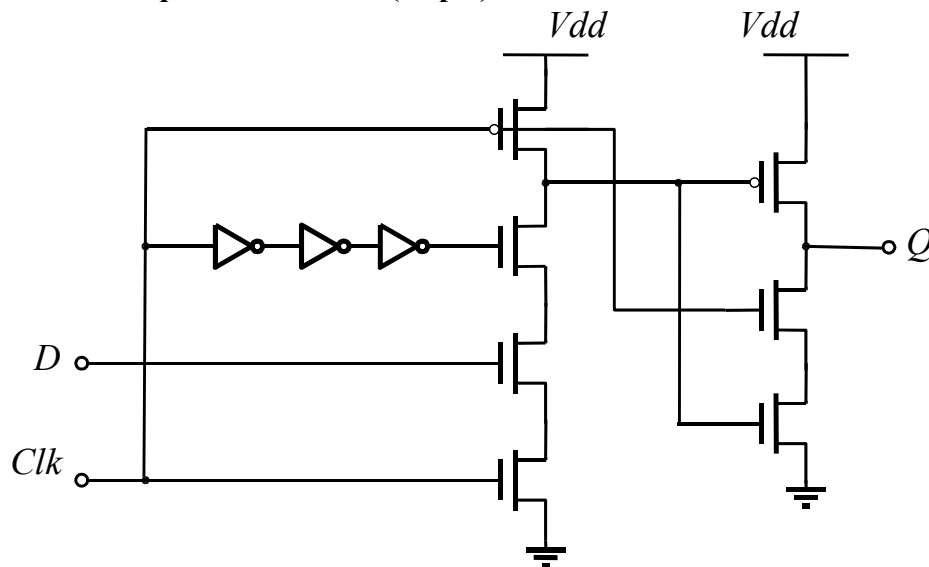

Chain structure   Tree structure

Compute the switching probabilities of the output, F, and internal nodes O1 and O2, for the chain and tree implementations of 4-input complementary CMOS AND gates, for the cases when input probabilities $P(A=1) = P(B=1) = P(C=1) = P(D=1)$ equal 0.25.

Problem 5. Sequential circuits. (10 pts)

a) (2 pts) Would the sequential circuit from the figure above be considered a latch, a master-slave latch pair or a pulse-triggered latch? Briefly explain your answer.

b) (5pts) All transistors in this circuit are unit-sized, with equivalent resistances R and gate capacitances C (ignore diffusion capacitances). Calculate the propagation delay t_{Clk-Q} for high-to-low and low-to-high transitions. Load on the output Q is equal $12C$. Ignore the signal slopes in delay calculation.

c) (3pts) This circuit does not strictly follow the rules for designing sequential logic discussed in the class. List three major problems in the operation of this circuit.

1. _____

2. _____

3. _____