PROBLEM 1. (22 pts) Inverter VTC and delay

A CMOS inverter at room temperature has a VTC as shown in Figure 1.

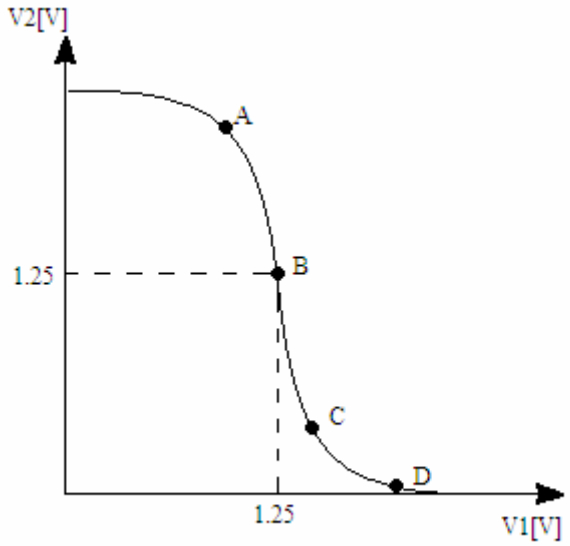


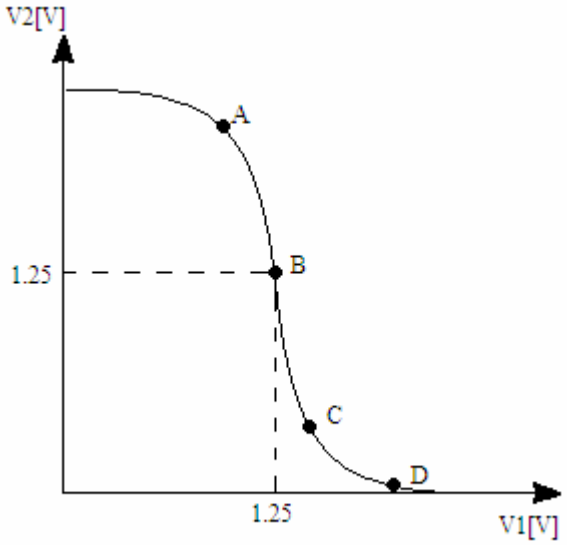
Figure 1

a) (8pts) Please indicate the region of operation of the PMOS and NMOS transistors for each point on the VTC

Point	V_{in}(V)	V_{out}(V)	PMOS	NMOS
A	0.95	2.4		
B	1.25	1.25		
C	1.50	0.15		
D	1.81	0.02		

b) (6pts) The input (gate) capacitance for this inverter equals its intrinsic (drain-bulk) capacitance $C_{input} = C_{intrinsic} = 3$ fF. In order to drive a large capacitive load, you would like to add a few more inverters (ignore the polarity of the output signal). What is the optimal number of inverters and their sizing that minimizes the delay of driving a capacitive load of $C_L = 150$ fF.

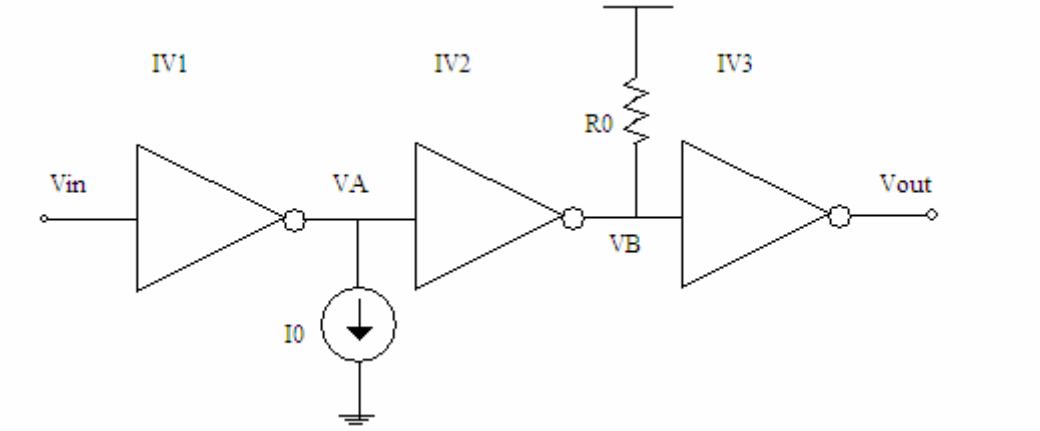
c) (4 pts) You decided to put your inverter into liquid Helium (Temperature = 4.2 K) to speed up its operation. The good news is that the inverter still works. And the unified model is still valid. But there are a few changes. First of all, k' for both NMOS and PMOS is increased by 50%; Also, the drain-bulk capacitance decreases to a very small number compared with the gate capacitance so that we can assume $\gamma = 0$. Based on the above facts, how does the VTC change and why? Draw it on the same diagram with the inverter at room temperature. Please briefly explain your answer.



d) (4 pts) Re-size the inverter chain for 4.2 K operation (repeat part b under the conditions from part c).

PROBLEM 2. (14 pts) CMOS logic gates.

A foundry has misprocessed the CMOS wafers and, as a result, the dielectric between metal 1 and diffusion layers accidentally leaks. This leakage can be modeled either as an ideal current source between the metal 1 wire and ground or as a resistance between metal 1 wire and VDD, as shown in Figure 1. We would like to investigate the impact of this dielectric leakage on the inverter properties. I_0 = 100μA, R_0 = 10kΩ.
All transistors are minimum length, NMOS transistors are 1μm wide and PMOS transistors are 2μm wide. Gate capacitances dominate the inputs, and diffusion capacitances dominate the outputs, $C_g = C_d$ = 2fF/μm.



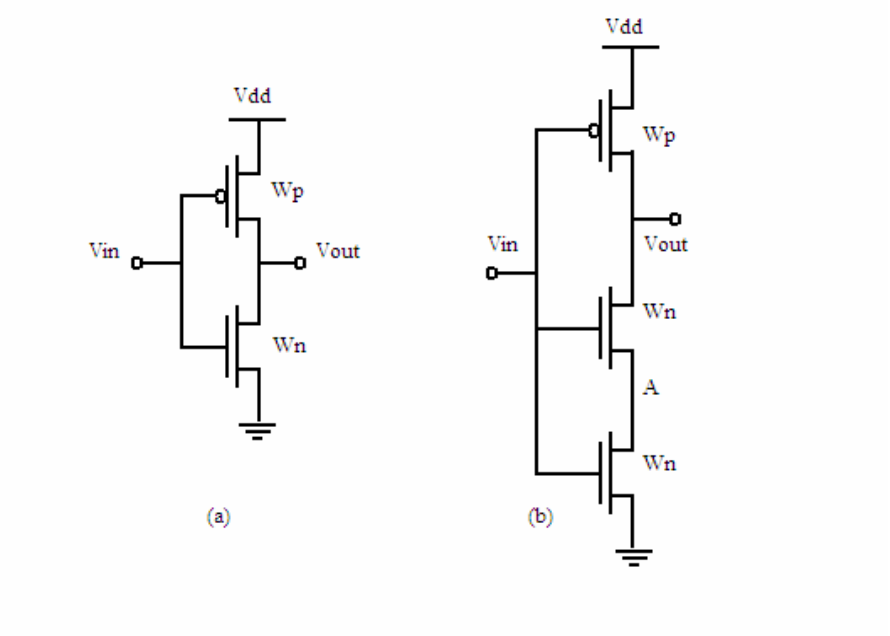
a) (4 pts) If the input (V_{in}) signal has full CMOS levels, what are the high and low signal levels at the output of the IV1 (V_A)?

b) (4 pts) Determine the high and low voltage levels at the output of the second inverter IV2 (V_B).

c) (6 pts) Determine the propagation delay of the second inverter IV2. You can ignore the effects of the slope on the delay.

PROBLEM 3. (14 pts) Propagation delay and power.

Two different designs of an inverter are shown in Figure 3. All transistors are minimum length L = 0.25µm, and for both inverters, W_P = 2µm, W_N = 1µm. Gate capacitances for all transistors equal diffusion capacitances $C_g = C_d$ = 2 fF/µ. All other capacitances can be ignored, as well as the diffusion capacitance at the node A and the body effect.



a) (4 pts) Find the ratio of $(t_{pLH})_a/(t_{pLH})_b$ for the inverters from Figure 3.a and 3.b when driving identical loads.

b) (4 pts) Find the ratio of $(t_{pHL})_a/(t_{pHL})_b$ for the inverters from Figure 3.a and 3.b when driving identical loads.

c) (4 pts) If inverters from Figure 3.a form one inverter chain of the length of 4, and inverters from Figure 3.b. form another chain of identical length, find the ratio of total power consumption between the two.

d) (2 pts) Inverter design from Figure 3.b. is used in practice for reduction in leakage power. What device effect is used to achieve this leakage reduction? Please briefly explain your answer.