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12:30-3:30pm

EECS 141: FALL 2008—FINAL EXAM

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

NMOS:
V_{Tn} = 0.2V, μ_n = 400 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, L=100nm, γ=λ=0
PMOS:
$|V_{Tp}|$ = 0.2V, μ_p = 200 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, L=100nm, γ =λ=0

NAME	Last Solutions First

GRAD/UNDERGRAD	

Problem 1: _____/ 16

Problem 2: _____/ 14

Problem 3: _____/ 24

Problem 4: _____/ 24

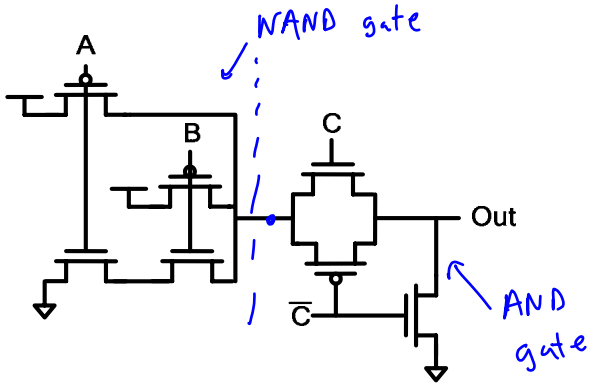
Problem 5: _____/ 18

Total: _____/ 96

PROBLEM 1: Logic Styles and LE (16 pts)

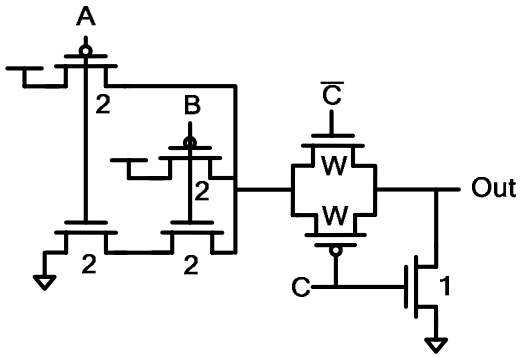
For this problem, you can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, $R_{sqp} = 20k\Omega/\square$, and that the transistors are quadratic (i.e., long-channel).

a) (3 pts) What logical function does the gate shown below implement?



$Out = (\bar{A} + \bar{B}) \cdot C$

b) (7 pts) Given the sizing shown below, what value of W would you use in order to make the worst-case LE of the C input equal to half the LE of the A and B inputs (i.e., $LE_C = \frac{1}{2} LE_A$)? What would be the LE of the C input in this case?



Note that the worst-case resistance of the stage is the same regardless of whether we are looking at the C, B, or A inputs. So, C_{in} for C must be 1/2 the C_{in} for A or B:

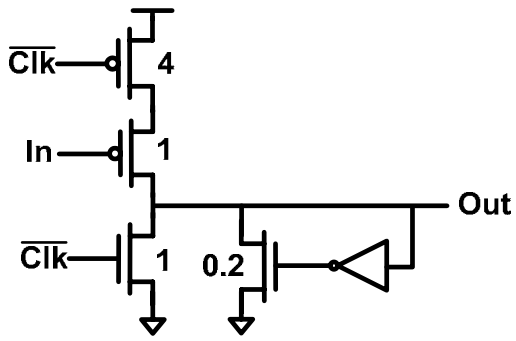
$C_{in_C} = \frac{1}{2} C_{in_A}$

$(W+1) = 2 \rightarrow W = 1$

$$LE_C = \frac{\left(\frac{1}{2} + \frac{1}{2} + 1\right) R_{sq} L \cdot 2C_g}{R_{sq} L \cdot 3C_g}$$

$LE_C = \frac{4}{3}$

c) (6 pts) During evaluation, what is the logical effort of the dynamic gate shown below from input In?



$$R_{pullup} = \frac{R_{sq,P}}{R_{sq,N}} \cdot \left(1 + \frac{1}{4}\right) = 2.5$$

$$R_{keeper} = \frac{1}{0.2} = 5$$

$$I_{pullup} \propto \frac{1}{2.5} - \frac{1}{5} = \frac{1}{5} \rightarrow R_{gate} = 5$$

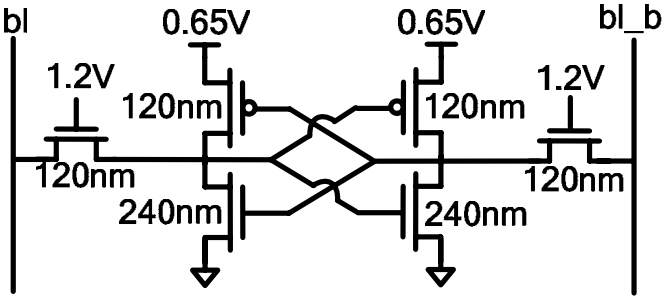
$$C_{gate} = 1$$

$$LE = \frac{R_{gate} C_{gate}}{R_{inv} C_{inv}} = \boxed{\frac{5}{3}}$$

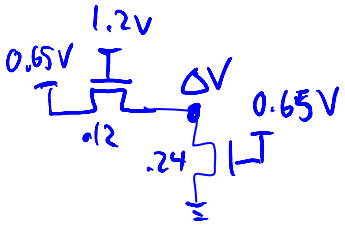
PROBLEM 2: SRAM Design (14 points)

For this problem you should use the velocity saturated transistor model.

a) **(8 pts)** Shown below is an SRAM cell during a read, where the power supply of the SRAM has been reduced to 0.65V while the V_{DD} of the wordline is 1.2V. Note that the bitlines have also been precharged to 0.65V. With the device sizing shown below, what is the read ΔV? (Hint: How much larger is I_{DSAT} for a transistor with V_{GS} = 1.2V than with V_{GS} = 0.65V?)



Read circuit:



$E_cL = \frac{2v_{sat}}{\mu} L = 0.5V \quad V_{TN} = 0.2V$

$$\frac{I_{DSAT}(V_{GS}=1.2V)}{I_{DSAT}(V_{GS}=0.65V)} = \frac{(1.2V-0.2V)^2/(1.2V-0.2V+0.5V)}{(0.65V-0.2V)^2/(0.65V-0.2V+0.5V)} \approx 3.13$$

So, even though access device is half as wide, its current would be higher than the pull-down device if $\Delta V \approx 0$. So, lets guess that both are in sat:

$$\frac{1}{2}\frac{(1.2V-\Delta V-0.2V)^2}{(1.2V-\Delta V-0.2V)+0.5V} = \frac{(0.65V-0.2V)^2}{(0.65-0.2V)+0.5V} \rightarrow \boxed{\Delta V \approx 278mV}$$

Check our guess:

$V_{GTaccess} = 1.2V - 278mV - 200mV = 722mV$

$V_{DSaccess} = 0.65V - 278mV = 372mV$

$V_{GTpd} = 0.65V - 0.2V = 450mV$

$V_{DSpd} = 278mV$

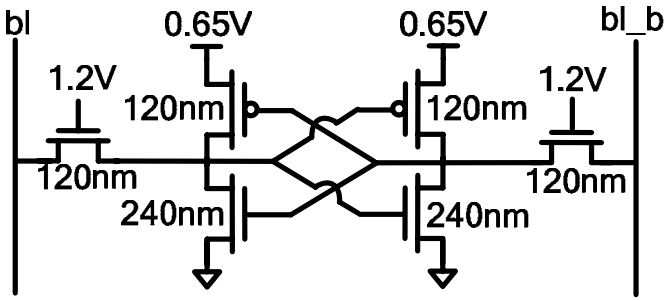
$V_{DSAT_a} = \frac{722mV \cdot 500mV}{722mV + 500mV} \approx 295mV$

access saturated ✓

$V_{DSAT_{pd}} = \frac{0.45V \cdot 0.5V}{0.45V + 0.5V} \approx 237mV$

pull down saturated ✓

b) **(6 pts)** Assuming that in your answer to part a) you calculated that the pull-down device is saturated, how much faster does the SRAM cell pull down the bitline when the wordline is driven to 1.2V compared to if the wordline was driven to only 0.65V? (Note that most of the credit on this problem will be given for finding the right regions of operation and setting up the equations.)



When $WL = 1.2V$:

$I_{pulldown} = I_{DSAT}$ of the pull-down device

$I_{pulldown} \propto 0.24 \cdot \frac{(0.65V - 0.2V)^2}{(0.65V - 0.2V) + 0.5V}$

When $WL = 0.65V$:

pull-down much bigger, so it should be in linear region.

0.65V
0.12 — 0.65V
ΔV
0.24 — 0.65V

Solve for ΔV:

$$0.12\mu m \cdot 1e7\,cm/s \; \frac{(0.65V - 0.2V - \Delta V)^2}{0.65V - 0.2V - \Delta V + 0.5V} = \frac{0.24\mu m}{0.1\mu m} \cdot 400\,cm^2/V\,sec\,(0.65V - 0.2V - \Delta V/2)\Delta V$$

$\hookrightarrow \Delta V \approx 52mV$

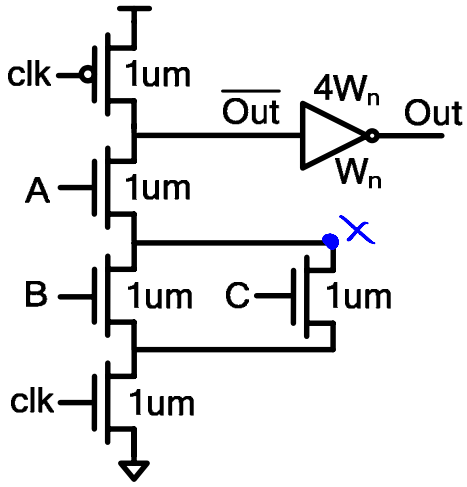
So, $$\frac{I_{pd}(WL = 1.2V)}{I_{pd}(WL = 0.65V)} = \frac{0.24\,(0.65V - 0.2V)^2/(0.65V - 0.2V + 0.5V)}{0.12\,(0.65V - 0.2V - 0.052V)^2/(0.65V - 0.2V - 0.052V + 0.5V)}$$

$$\boxed{\frac{I_{pd}(WL = 1.2V)}{I_{pd}(WL = 0.65V)} \approx 2.417}$$

PROBLEM 3: Dynamic Logic Design (24 pts)

For this problem, you can assume that $V_{DD} = 1.2V$, $C_G = 2fF/\mu m$, and $C_D = 1fF/\mu m$.

a) (6 pts) In the domino gate shown below, what is the minimum W_n necessary to ensure that the gate does not fail due to charge sharing? You can assume that with the sizing shown, the V_{IH} of the inverter is $¾ \cdot V_{DD}$, and that none of the source/drain regions have been shared.



Cap on node X:

$C_X = C_{DC} + C_{DB} + C_{DA} + C_{GA}$

$= 3\mu m \cdot 1fF/\mu m + 1\mu m \cdot 2fF/\mu m$

$= 5fF$

Cap on node $\overline{Out}$:

$C_{\overline{out}} = C_{DA} + C_{Dpre} + 5W_N C_G$

$= 2fF + 10fF/\mu m \cdot W_N$

Charge sharing: $V_{DD} \cdot C_{\overline{out}} = V_{new}(C_{\overline{out}} + C_X)$

$V_{new} = \frac{C_{\overline{out}}}{C_{\overline{out}} + C_X} \cdot V_{DD}$

To meet V_{IH} of inverter: $V_{new} > \frac{3}{4} V_{DD}$

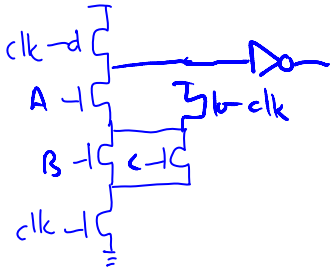
$$\frac{2fF + 10fF/\mu m \cdot W_N}{2fF + 10fF/\mu m \cdot W_N + 5fF} > \frac{3}{4}$$

$2fF + 10fF/\mu m\, W_N \geq 5.25\,fF + 7.5\,fF/\mu m\, W_N$

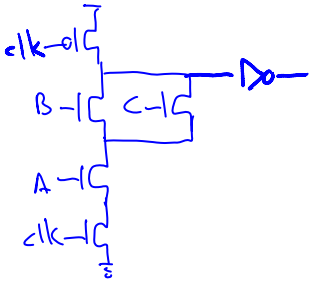
$\boxed{W_N \geq 1.3\mu m}$

b) (6 pts) Other than changing W_n, the sizes of the transistors in the dynamic gate, or adding a keeper, what else can change in the gate from part a) in order to mitigate the charge sharing issue? You should explain your changes and draw a new transistor-level schematic of the gate (no sizing necessary). To receive full credit on this problem, you should identify two independent changes; if you identify three changes you will receive bonus credit.

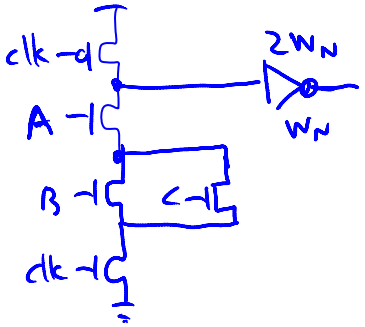
(1) Pre-charge the internal node:



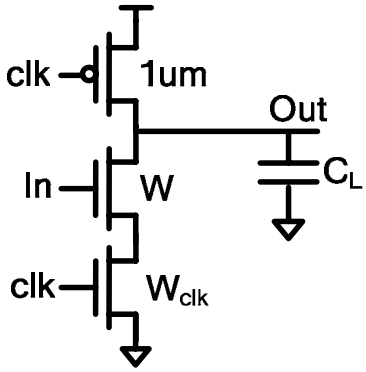
(2) Re-order the gate to increase C_{out}:



(3) Reduce the skew of the inverter to decrease V_{IH} (doesn't reduce charge sharing, but reduces its impact on the output).



c) (2 pts) On the evaluation edge, what is the delay of the dynamic gate shown below as a function of $R_{sq,n}$, C_L, W, and W_{clk}? You can assume that $C_D = 0$ and ignore slope effect.



$$t_p = \ln(2) R_{sqN} \cdot L \cdot \left(\frac{1}{W} + \frac{1}{W_{clk}} \right) \cdot C_L$$

d) (2 pts) Assuming that In has an activity factor of $\alpha_{0\to1}$, how much power is consumed due to driving In? How about due to driving clk? You should provide your answers in terms of W, W_{clk}, $\alpha_{0\to1}$, C_G, V_{DD}, and *f*.

$$P_{In} = \alpha_{0\to1} C_G \cdot W V_{DD}^2 f$$

$$P_{clk} = C_G (W_{clk} + 1\mu m) V_{DD}^2 f$$

e) (8 pts) Increasing the size of the evaluation transistor (i.e., increasing W_{clk}) speeds up the dynamic inverter, but costs power. Using the results from parts c) and d), can you find an optimal W_{clk}/W?

"Optimal" here can only mean that we are spending just the right amount of power for a given delay (or hitting the best delay for a given power). That means we should be looking at sensitivities of W and W_{clk} and trying to balance them.

$$\frac{\partial t_p}{\partial W} = -\frac{\ln(2) R_{sqN} L C_L}{W^2} \qquad \frac{\partial t_p}{\partial W_{clk}} = -\frac{\ln(2) R_{sqN} L C_L}{W_{clk}^2}$$

$$\frac{\partial P}{\partial W} = \alpha_{0\to1} C_g V_{DD}^2 f \qquad \frac{\partial P}{\partial W_{clk}} = C_g V_{DD}^2 f$$

$$S_W = -\frac{\alpha_{0\to1} C_g V_{DD}^2 f}{\ln(2) R_{sqN} L C_L} \cdot W^2 \qquad S_{W_{clk}} = -\frac{C_g V_{DD}^2 f}{\ln(2) R_{sqN} L C_L} \cdot W_{clk}^2$$

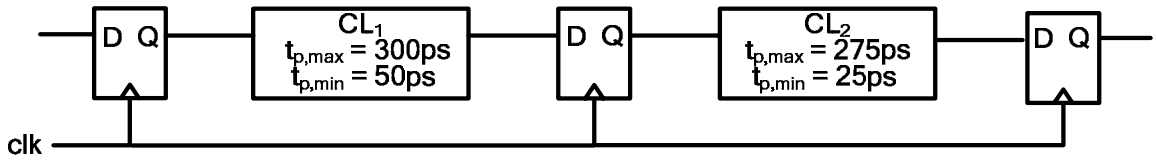
$$S_W = S_{W_{clk}}$$

$$-\left(\frac{C_g V_{DD}^2 f}{\ln(2) R_{sqN} L C_L}\right) \alpha_{0\to1} W^2 = -\left(\frac{C_g V_{DD}^2 f}{\ln(2) R_{sqN} L C_L}\right) W_{clk}^2$$

$$\hookrightarrow \boxed{\frac{W_{clk}}{W} = \sqrt{\alpha_{0\to1}}}$$

PROBLEM 4: Timing and Clock Distribution (24 points)

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk\text{-}q}$ = 50ps, t_{setup} = 25ps, and t_{hold} = 25ps. You can assume that the clock has no jitter.



a) (6 pts) What is the minimum clock cycle time for this pipeline? Are there any minimum delay violations?

Min. cycle: CL_1 has largest $t_{p,max}$, so:

$$t_{clk\text{-}q} + t_{p,max1} + t_{setup} < T_{cycle}$$

$$50ps + 300ps + 25ps < T_{cycle}$$

$$\boxed{T_{cycle} > 375ps}$$

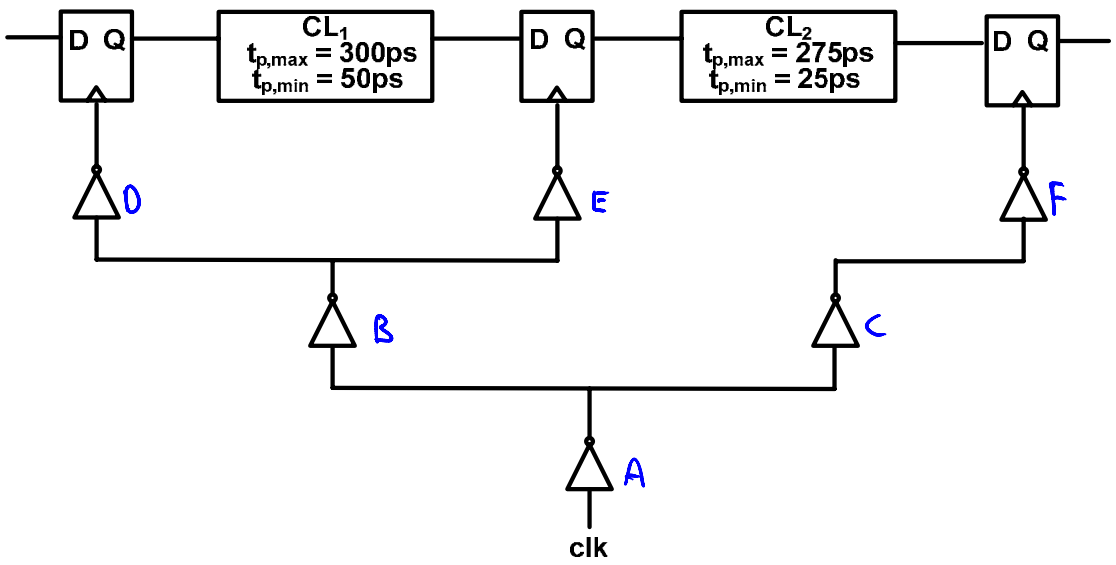
Min. delay: CL_2 has smallest $t_{p,min}$, so:

$$t_{clk\text{-}q} + t_{p,min2} > t_{hold}$$

$$50ps + 25ps > 25ps$$

$$50ps > 0ps \checkmark$$

↳ No hold time problem.



b) (4 pts) Now we'll include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 50ps, but that each inverter's delay varies randomly by +/-20%, now what is the minimum clock cycle time?

Each inverter delay varies by ±10ps. CL_1 has largest max delay, but since only picks up skew from inverters D and E (whereas path through CL_2 has skew from B, E, C, and F), need to check which one is the most critical.

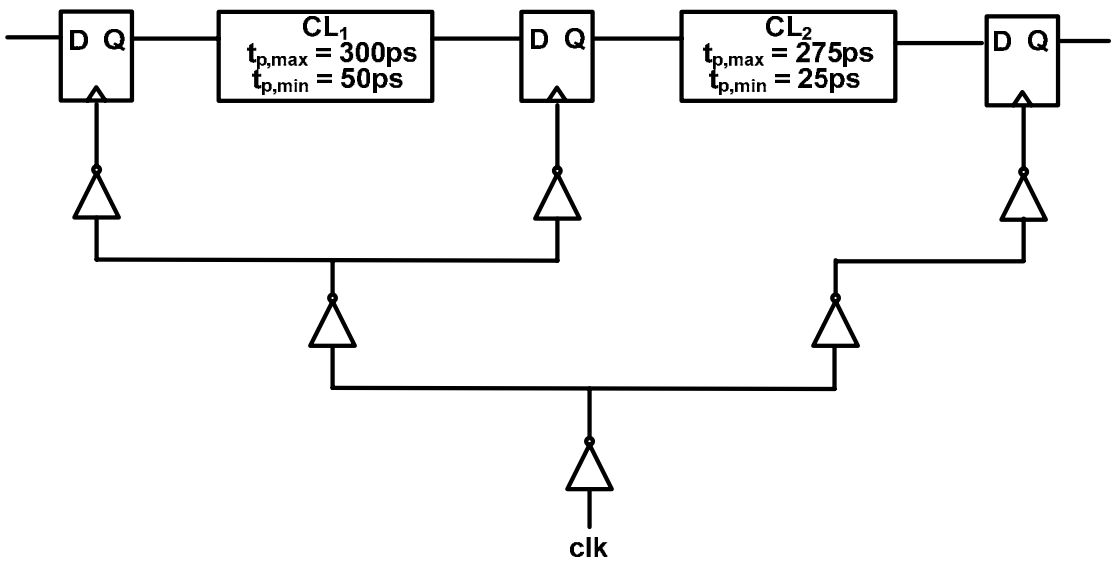
$t_{p,max_1} + 2\Delta t_{INV} = 300ps + 20ps = 320ps$

$t_{p,max_2} + 4\Delta t_{INV} = 275ps + 40ps = 315ps$

So, CL_1 is still critical:

$$t_{clk\text{-}q} + t_{p,max_1} + t_{setup} + 2\Delta t_{INV} < T_{cycle}$$

$$\boxed{T_{cycle} < 395ps}$$



c) (4 pts) Under these same conditions (i.e., 50ps nominal inverter delay, +/-20% delay variation), can this pipeline fail any minimum delay constraints?

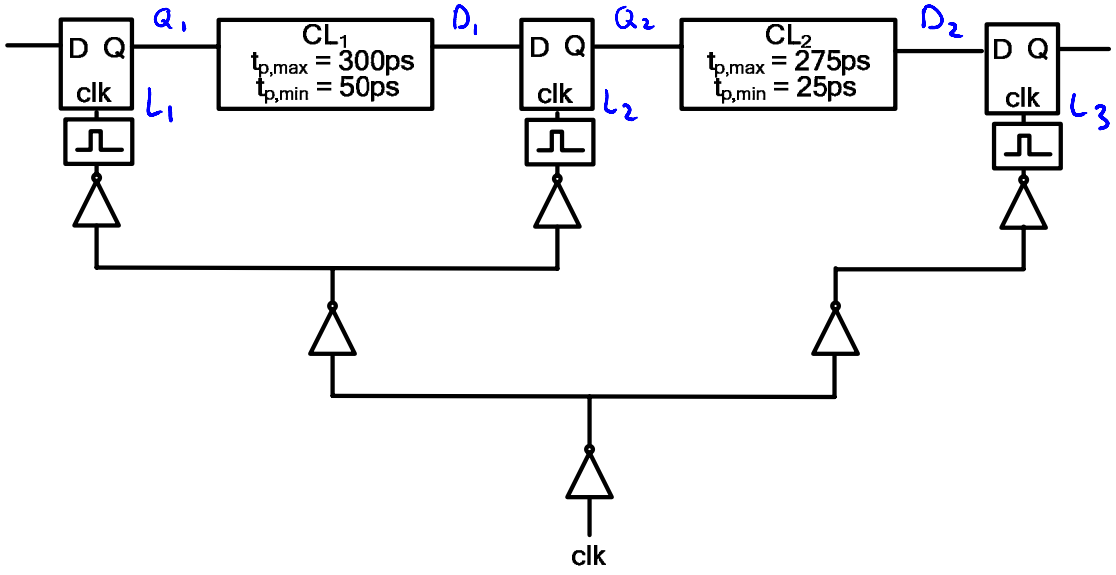
Path through CL_2 has smallest $t_{p,min}$ and most skew, so that's clearly where we need to worry about failure.

$$t_{clk-q} + t_{p,min2} > t_{hold} + 4\Delta t_{inv}$$

$$50ps + 25ps > 25ps + 40ps$$

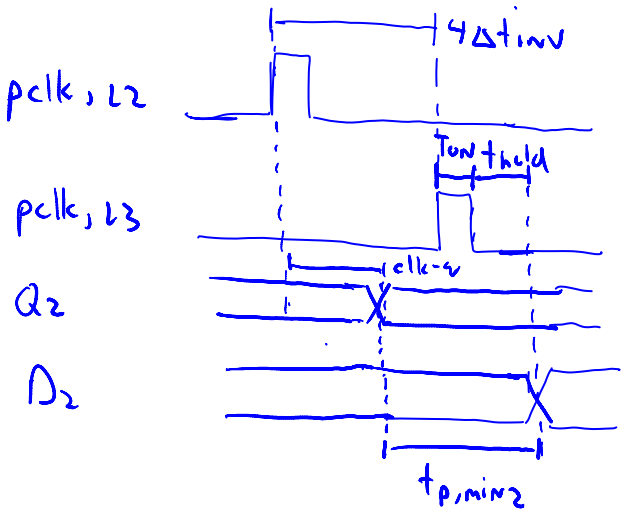
$$10ps > 0ps \quad \checkmark$$

↳ No hold time violation.



d) (10 pts) If we replace the flip flops by pulsed latches with the same $t_{clk\text{-}q}$, t_{setup}, and t_{hold} as the flip-flops, and with $t_{d\text{-}q} = t_{clk\text{-}q} + t_{setup}$, can the minimum cycle time of the pipeline be reduced without potentially failing a minimum delay constraint? If so, how wide must the pulses be, and what is the new minimum cycle time? If not, explain which path fails the minimum delay constraint.

Find max pulse width without hold time:

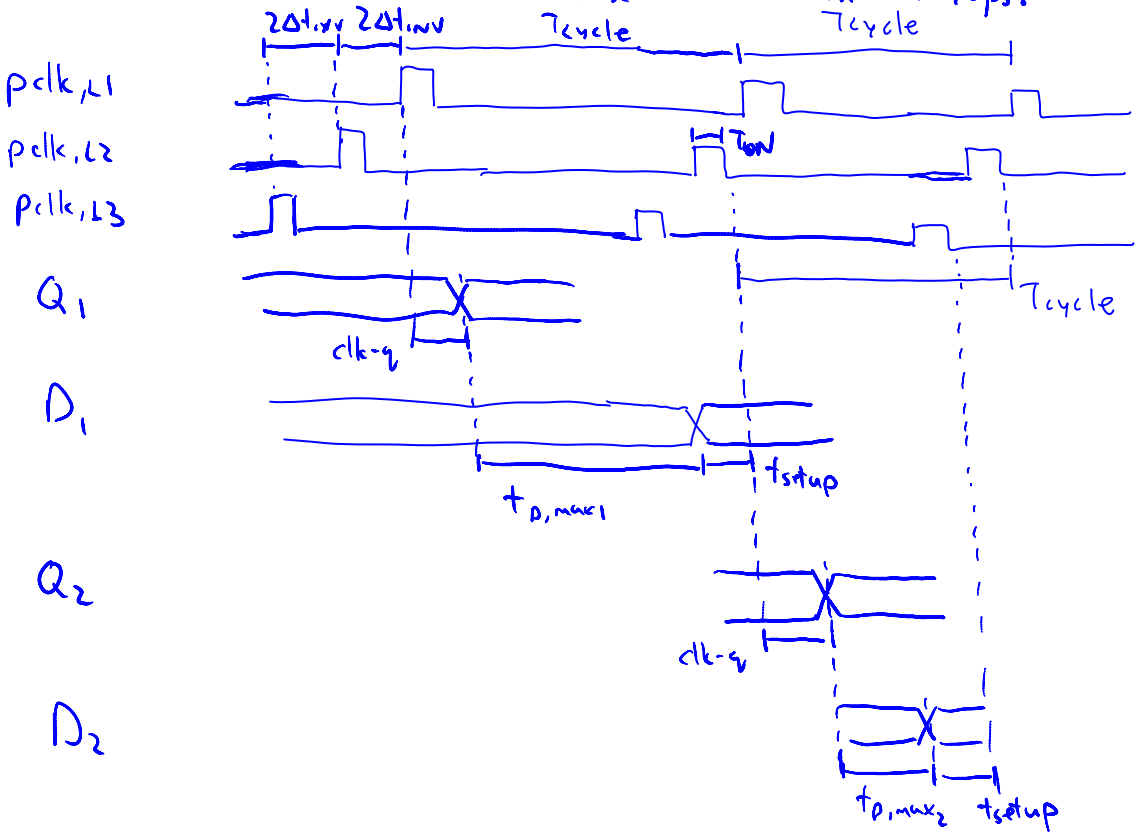


$$t_{clk\text{-}q} + t_{p,min2} \geq 4\Delta t_{inv} + T_{ow} + t_{hold}$$

$$T_{ow} \leq 50ps + 25ps - 40ps - 25ps$$

$$T_{ow} \leq 10ps$$

For cycle time, look at worst-case skew with $T_{ON} = 10ps$:



For path through CL_1: $t_{clk-q} + t_{p,max_1} + t_{setup} < T_{cycle} - 2\Delta t_{inv} + T_{ON}$

$$\boxed{T_{cycle} > 385ps}$$

Check that path through CL_2 is still OK:

$$t_{clk-q} + t_{p,max_2} + t_{setup} < T_{cycle} - 2\Delta t_{inv}$$

$350ps < 365ps$ ✓

↳ CL_2 OK. (OK even if needed to be before L3 ↑.)

* If you get the right T_{cycle}, you will receive full credit.
* If you check that the CL_2 path is still OK under these conditions, you will receive bonus points.

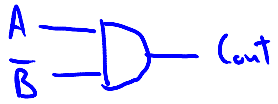
PROBLEM 5: Arithmetic (18 pts)

In this problem we will look at designing a comparator whose output C_{out} = 1 whenever A > B, where A and B are unsigned binary numbers. Throughout this problem you can assume that you have both the true and complement versions of the inputs available to you.

a) (2 pts) If A and B are both only a single bit, draw a gate-level schematic (i.e., no transistors) showing how you would compute C_{out}.

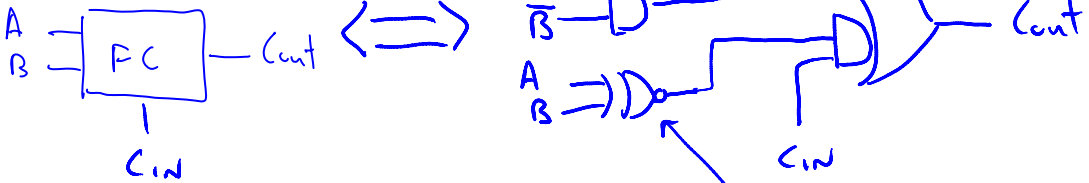
If A=1 and B=0, A>B.

So:



b) (5 pts) Now assume that A and B are both two bit numbers – i.e., we have inputs $A_{1:0}$ and $B_{1:0}$. To compare between A_0 and B_0 we can use the "half comparator" circuit you drew in part a). Draw a gate level schematic showing how you would implement a "full comparator" and use it to calculate the final C_{out}.

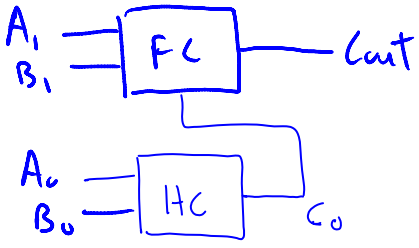
A	B	Cout
0	0	C_{IN}
0	1	0
1	0	1
1	1	C_{IN}



Two-bit comparator:

This can also be replaced with

(see next page)



c) (5 pts) Notice that these comparators have several characteristics that are very similar to adders. As a function of A and B, define new P (propagate) and G (generate) signals that are appropriate for comparators, and then write the logic equation that gives the C_{out} for a particular bit using P, G, and C_{in}.

Look at truth table again:

A	B	Cout	P	G
0	0	Cin	1	0
0	1	0	0	0
1	0	1	X	1
1	1	Cin	1	0

(Never use intermediate Couts, so it doesn't matter what P is when G=1)

$G = A \cdot \bar{B}$ $\quad P = A + \bar{B}$

or

$P = \bar{A} \cdot \bar{B} + A \cdot B = \overline{A \oplus B}$

$C_{out} = G + P \cdot C_{in}$

d) (6 pts) Given your definitions from part c), sketch a block diagram showing how you can implement an 8-bit "carry lookahead" comparator using the PG block shown below.