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6:30-8:00pm

EECS 141: FALL 2009—MIDTERM 2

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

NMOS:
V_{Tn} = 0.2V, μ_n = 400 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, λ = 0
PMOS:
$|V_{Tp}|$ = 0.2V, μ_p = 200 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, λ = 0

NAME	Last Solutions First

GRAD/UNDERGRAD	

Problem 1: _____/ 14

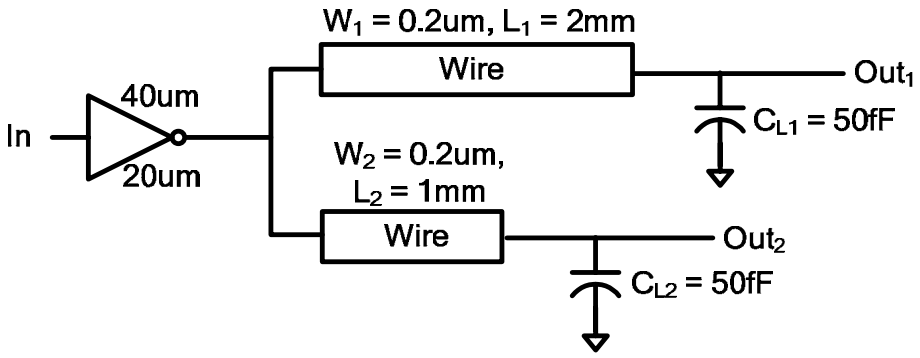
Problem 2: _____/ 30

Problem 3: _____/ 14

Total: _____/ 58

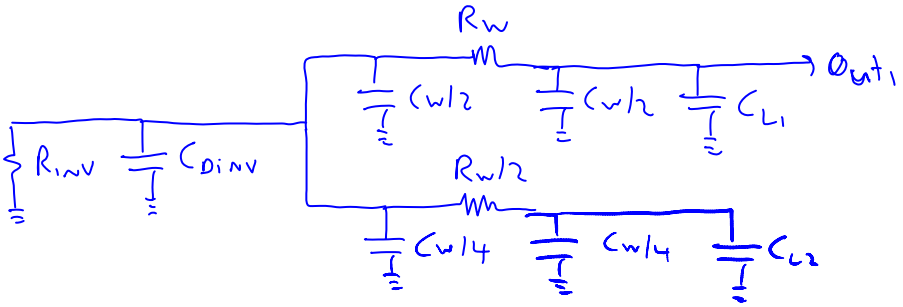
PROBLEM 1. (14 pts) Wires and Delay

For this problem, you should assume that all of the transistors are minimum channel length (L=0.1µm) and have the following characteristics: C_G = 2fF/µm, C_D = 1fF/µm, and $R_{sqn} = R_{sqp}/2$ = 15kΩ/□. For the wires, you should assume that C_{wpp} = 0.1fF/µm^2, $C_{wfringe}$ = 0.05fF/µm/edge, and R_{sqw} = 0.1Ω/□



a) (8 pts) What is the ramp delay of the circuit shown above from In to Out_1?

Draw the RC model:



$R_{INV} = R_{sqn} \cdot \frac{L}{W_N} = 75\Omega$

$C_{DINV} = (W_N + W_P) \cdot C_D = 60fF$

$C_W = W_1 \cdot L_1 \cdot C_{wpp} + 2L_1 C_{wfringe} = 240fF$

$R_W = R_{sqw} \cdot \frac{L_1}{W_1} = 1k\Omega$

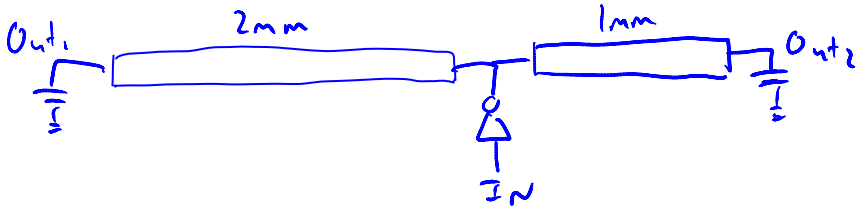
$t_{pout_1} = R_{INV}(C_{DINV} + C_W + C_{L2}) + (R_{INV} + R_W)(\frac{C_W}{2} + C_{L1})$

$t_{pout_1} = 26.25ps + 182.75ps \rightarrow \boxed{t_{pout_1} = 209ps}$

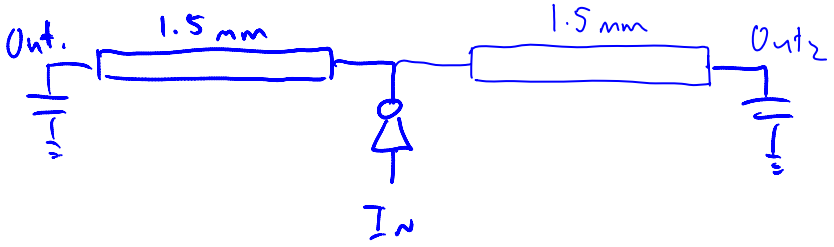
b) (6 pts) Now let's assume that this circuit is actually a part of the chip's clock distribution network, and hence we want to make sure that for any value of V_{DD}, the delay from In to Out_1 is always exactly the same as the delay from In to Out_2. Draw a new circuit that achieves this goal; you can modify anything in the original circuit except for the values of C_{L1} and C_{L2} and the total length of the wires (i.e., $L_1 + L_2 = 3mm$).

Only way to do this robustly is to make the circuit symmetric – i.e., place the driver in the center of the total wire length.

Old design:

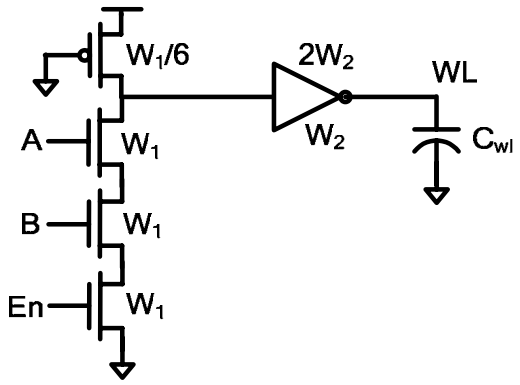


New design:



PROBLEM 2. (30 pts) Decoder Energy-Delay Tradeoffs.

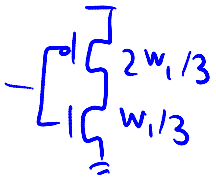
This problem will deal with the final decoder circuit shown below. This final decoder is used inside of a 32x32 SRAM, where A and B are outputs from the predecoders. Throughout this problem you can assume that C_G = 2fF/μm, C_D = 0, $R_{sqn} = R_{sqp}/2$ = 10kΩ, that the transistors are long-channel from the standpoint of calculating logical effort, and that subthreshold leakage current is negligible.



a) **(6 pts)** In units of t_{inv} and as a function of W_1, W_2, and C_{wl}/C_G, what is the delay of the final decoder from A or B rising to WL rising?

$LE_{NAND3} = \frac{R_{gate} C_{gate}}{R_{inv} C_{inv}}$

ref inv:



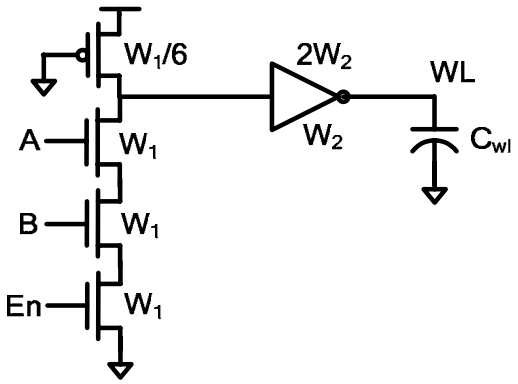
$\frac{C_{gate}}{C_{inv}} = 1$

$\frac{1}{R_{gate}} = \frac{W_1}{3R_{sq}L} - \frac{W_1}{12R_{sq}L} = \frac{W_1}{3R_{sq}L} \cdot \left(1 - \frac{1}{4}\right) = \frac{W_1}{4R_{sq}L}$

$\hookrightarrow \frac{R_{gate}}{R_{inv}} = \frac{4}{3}$ $\quad LE = \frac{4}{3}$

$t_p = \frac{4}{3} \cdot \frac{3W_2}{W_1} \cdot t_{inv} + \frac{C_{wl}}{3W_2 C_G} \cdot t_{inv}$

$$t_p = \left(\frac{4W_2}{W_1} + \frac{C_{wl}/C_G}{3W_2}\right) \cdot t_{inv}$$



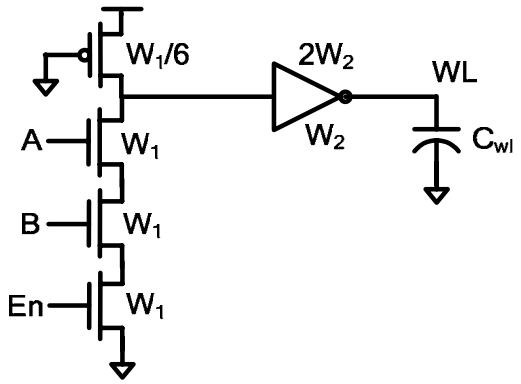
b) **(11 pts)** Assuming that the SRAM operates at a clock frequency of *f*, what is the average power consumed by this final decoder? You do not need to include the power consumed by driving the A, B, and En inputs, and you can assume that the En signal is a clock, but that it is only high 20% of the clock cycle. For simplicity you can also assume that the V_{OL} of the ratioed gate is ~0V, and that the I_{DSAT} of a PMOS transistor is equal to $V_{DD}/(R_{sqp}*L/W)$.

* First think about activity factor; SRAM has 32 wordlines, so one wordline is high 1/32 of the time. However, since En is a clock, every time the wordline goes high it is guaranteed to go back low. So $\alpha_{WL} = 1/32$; this is also the activity factor at the output of the ratioed gate.
* We also need to remember that the ratioed gate draws static current whenever its output is low. This only happens (on average) once every 32 cycles, and only while En is high (i.e., 20% of the clock cycle)
* So:

$$P_{avg} = \alpha_{WL} \cdot C_L V_{DD}^2 f + \alpha_{WL} \cdot 3W_2 (6 V_{DD}^2 f + 1/5 \cdot \alpha_{WL} \cdot I_{ratioed} \cdot V_{DD}$$

$$P_{avg} = \alpha_{WL} \cdot V_{DD}^2 f \left(C_L + 3W_2(6) + 1/5\, \alpha_{WL} V_{DD} \cdot \frac{V_{DD} \cdot W_1/6}{2 R_{sqp} \cdot L} \right.$$

$$\boxed{P_{avg} = \alpha_{WL} \cdot V_{DD}^2 \cdot \left(C_L \cdot f + 3W_2 C_G \cdot f + \frac{W_1}{60} \cdot \frac{1}{L R_{sqp}} \right)}$$



c) **(6 pts)** With f = 1GHz, W_1 = 2µm, W_2 = 2µm, and C_{WL} = 50fF and as a function of V_{DD} and t_{inv}, what are the sensitivities S_{W1} and S_{W2}, where S_x = (∂Power/∂x)/(∂Delay/∂x)?

$$\frac{\partial P}{\partial W_1} = \alpha_{WL} V_{DD}^2 \cdot \left(\frac{1}{60\, L R_{sq,N}}\right)$$

$$\frac{\partial t_p}{\partial W_1} = -\frac{4W_2}{W_1^2} \cdot t_{inv}$$

$$S_{W_1} = -\frac{\alpha_{WL} V_{DD}^2}{t_{inv}} \cdot \frac{W_1^2}{240\, W_2 L R_{sq,N}}$$

$$\boxed{S_{W_1} = -\frac{1}{120k\Omega} \cdot \frac{\alpha_{WL} \cdot V_{DD}^2}{t_{inv}}}$$

$$\frac{\partial P}{\partial W_2} = \alpha_{WL} V_{DD}^2 \cdot (3 C_G f)$$

$$\frac{\partial t_p}{\partial W_2} = \left(\frac{4}{W_1} - \frac{C_L/C_G}{3W_2^2}\right) \cdot t_{inv}$$

$$S_{W_2} = \alpha_{WL} \frac{V_{DD}^2}{t_{inv}} \cdot \frac{3 C_G f}{\frac{4}{W_1} - \frac{C_L/C_G}{3W_2^2}}$$

$$S_{W_2} = \left(\frac{3 \cdot 2fF/\mu m \cdot 1GHz}{2\,\mu m^{-1} - \frac{25}{12}\mu m^{-1}}\right) \cdot \alpha_{WL} \frac{V_{DD}^2}{t_{inv}}$$

$$\boxed{S_{W_2} \approx -\frac{1}{13.89k\Omega} \cdot \alpha_{WL} \frac{V_{DD}^2}{t_{inv}}}$$

d) **(7 pts)** If you wanted to decrease the power consumption of the final decoder while maintaining the same delay, how would you modify the sizing of the gates? Please be as specific as possible and be sure to explain your answer.

Both sensitivities point in the "right" direction - i.e., that if we change those variables we will be sacrificing delay to reduce power. However, the absolute magnitude of S_{W_2} is about 10 times larger than that of S_{W_1}. This means that we should decrease W_2 and then slightly increase W_1 to make up for the increased delay.

In fact, if you work out the true optimal solution (by fixing the delay to the same value and setting the sensitivities equal), you can show that the best sizing for this particular delay is

$W_1 \approx 2.04$ and $W_2 \approx 1.8$

PROBLEM 3. Scaling (14 points)

You recently designed a microprocessor in a 65nm technology with V_{DD} = 1.2V and V_T = 0.35V that runs at 2GHz and consumes a total power of 1W, where 750mW is dynamic power and 250mW is due to subthreshold leakage. In this problem we will look at some of the choices available to us if we were to scale the design to a 45nm technology. Throughout the problem, you should assume that leakage current is modeled by $WI_0e^{(-V_T/38mV)}$, where I_0 is the same in both the 65nm and 45nm technologies.

a) **(7 pts)** Using the full scaling model and assuming velocity saturated devices, what would be the new operating frequency, supply voltage, and power consumption of the chip in the 45nm technology?

$S = \frac{45nm}{65nm}$ $\quad V_{DD,new} = S V_{DD}$ $\quad \boxed{V_{DD,new} \approx 0.83V}$

$I_{DSAT} \propto W v_{sat} C_{ox} \frac{(V_{DD}-V_T)^2}{(V_{DD}-V_T)+\xi_c L} \propto S$

$C_L \propto WLC_{ox} \propto S$ $\quad t_p \propto \frac{C_L V_{DD}}{I_{DSAT}} \propto S$

$f_{clk} \propto \frac{1}{t_p} \propto \frac{1}{S} \rightarrow \boxed{f_{clk,new} \approx 2.89\,GHz}$

$P_{dyn} \propto C_L V_{DD}^2 f \propto S \cdot S^2 \cdot \frac{1}{S} \propto S^2 \rightarrow P_{dyn,new} \approx 359.47mW$

$P_{leak} \propto V_{DD} W e^{-V_T/38mV}$ $\quad \frac{P_{leak,new}}{P_{leak,old}} \propto S \cdot S \cdot \frac{e^{-SV_T/38mV}}{e^{-V_T/38mV}}$

$P_{leak,new} \approx 8.1544 \cdot P_{leak} \approx 2.04W$

$\boxed{P_{avg,new} \approx 2.4W}$

b) **(7 pts)** Now let's assume that in moving to the 45nm technology we leave V_{DD} = 1.2V and V_T = 0.35V. Still with velocity saturated devices and assuming that ξ_{crit} = 5V/μm, now what is the new operating frequency and power consumption of the chip?

$C_L \propto S$

$$I_{DSAT} \propto W v_{sat} C_{ox} \frac{(V_{DD}-V_T)^2}{(V_{DD}-V_T)+\xi_c L}$$

$$\frac{I_{DSAT,new}}{I_{DSAT,old}} = S \cdot \frac{1}{S} \cdot \frac{(V_{DD}-V_T)+\xi_c 65nm}{(V_{DD}-V_T)+\xi_c 45nm} = 1.093$$

$$t_{p,new} \propto \frac{C_L V_{DD}}{I_{DSAT}} \propto \frac{S}{1.093} \propto 0.633$$

$$\boxed{f_{new} \approx 3.16\,GHz}$$

$$P_{dyn,new} \propto C_L V_{DD}^2 f_{new} \propto S \cdot \frac{1.093}{S}$$

$$P_{dyn,new} = 819.75\,mW$$

$$P_{leak,new} \propto V_{DD} \cdot W I_0 e^{-V_T/38mV} \propto S$$

$$P_{leak,new} \approx 173.08\,mW$$

$$\boxed{P_{avg,new} = 992.83\,mW}$$