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Wednesday, December 15, 2010
8:00-11:00am

EECS 141: FALL 2010—FINAL EXAM

For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):

NMOS:
V_{Tn} = 0.2V, μ_n = 400 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, L=100nm, γ=λ=0
PMOS:
$|V_{Tp}|$ = 0.2V, μ_p = 200 cm^2/(V·s), C_{ox} = 1.125 μF/cm^2, v_{sat} = 1e7 cm/s, L=100nm, γ =λ=0

NAME	Last First

GRAD/UNDERGRAD	

Problem 1: _____/ 10

Problem 2: _____/ 18

Problem 3: _____/ 15

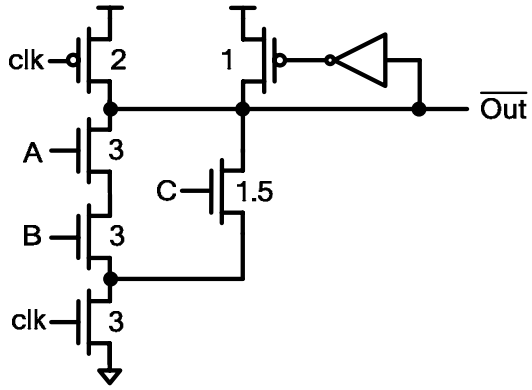
Problem 4: _____/ 26

Problem 5: _____/ 21

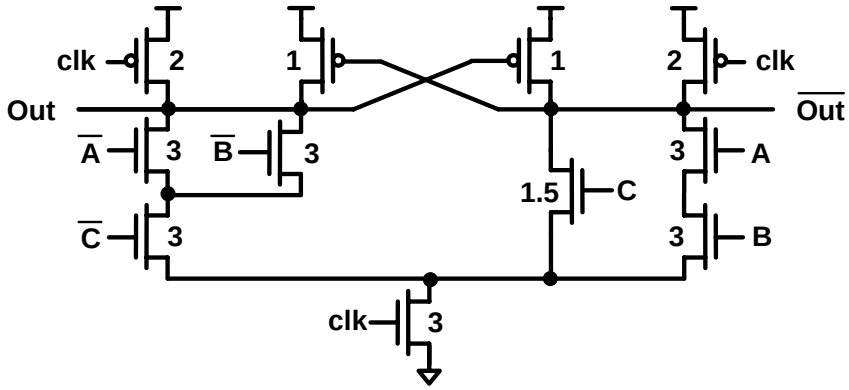
Total: _____/ 90

PROBLEM 1: Logic Styles (10 points)

a) (5 pts) Assuming $R_{sqp} = 2*R_{sqn}$ and quadratic devices, what is the logical effort of the dynamic gate shown below from the A input?

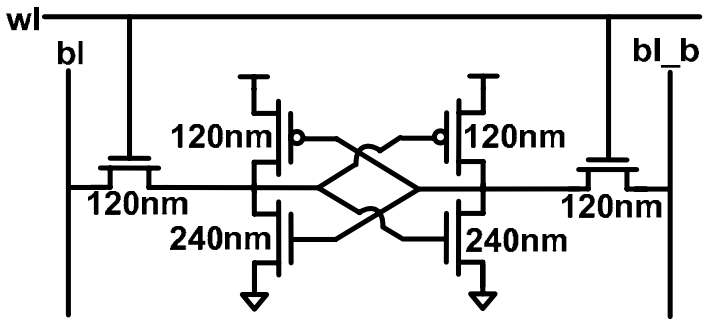


b) (5 pts) For the dual rail domino version of the same gate shown below, now what is the logical effort from the A input?



PROBLEM 2: SRAM Design (18 pts)

For this problem we will be looking at a 128x128 SRAM (i.e., each wordline drives 128 cells, and each bitline has 128 cells on it), with each cell shown below. The cell's layout is 2μm tall and 2.5μm wide, and both the wordline and bitline wires are 0.1μm wide. You can assume that $C_G = C_D = 2fF/\mu m$, $R_{sqn} = 10k\Omega/\square$, $R_{sqp} = 20k\Omega/\square$, and that for the wordline and bitline wires, $R_w = 0.1\Omega/\square$ and $C_w = 0.2fF/\mu m$.

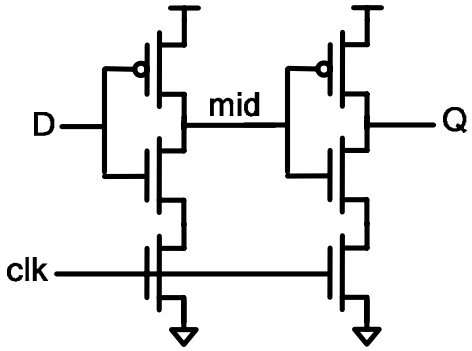


a) (5 pts) For this SRAM, what is the total capacitance on each wordline? What is the total capacitance on each bitline?

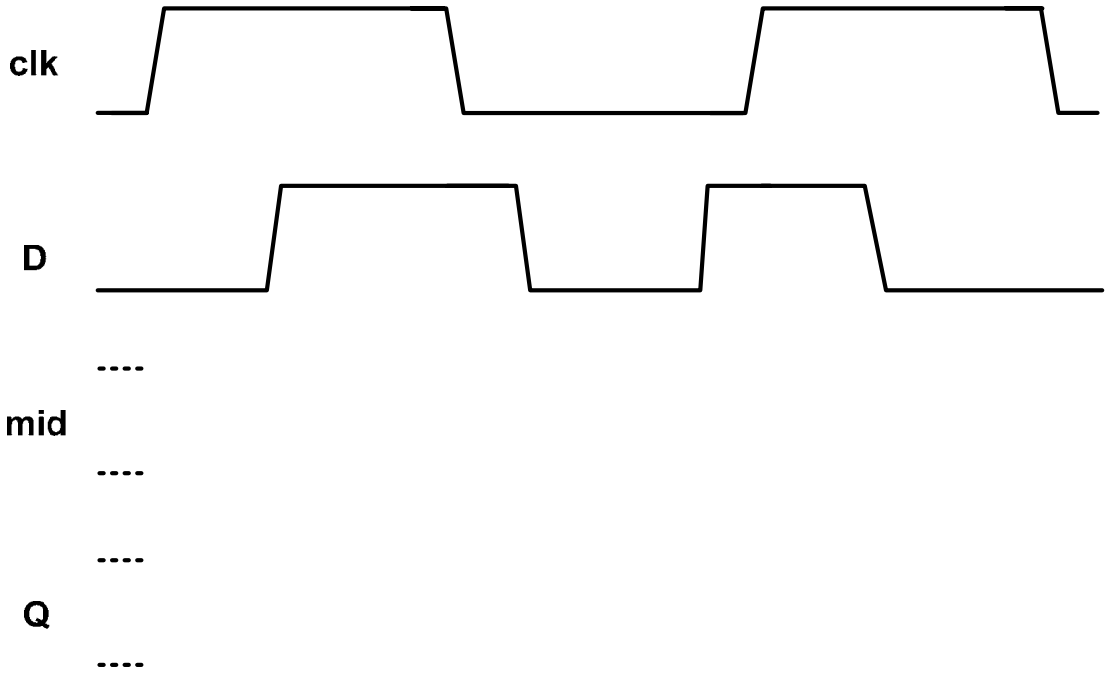
b) (4 pts) Assuming this SRAM works at 1GHz and V_{DD}=1.2V, how much dynamic power is consumed due to the capacitance of the wordlines and bitlines?

c) (9 pts) Now let's see what happens when we change the size of the SRAM array. Assuming that the final gate driving the wordline is always an inverter sized to have a fanout of four, how many SRAM cells can you place on each wordline before the delay caused by the resistance of the wordline wire is equal to the delay caused by the resistance of the inverter that drives the wordline?

PROBLEM 3: Sequential Elements (15 points)
In this problem we will be examining the latch shown below.



a) (4 pts) Assuming the latch is ideal (i.e., has no delay, zero setup/hold time, etc.), fill in the waveforms for mid and Q given the clock and data inputs shown below.

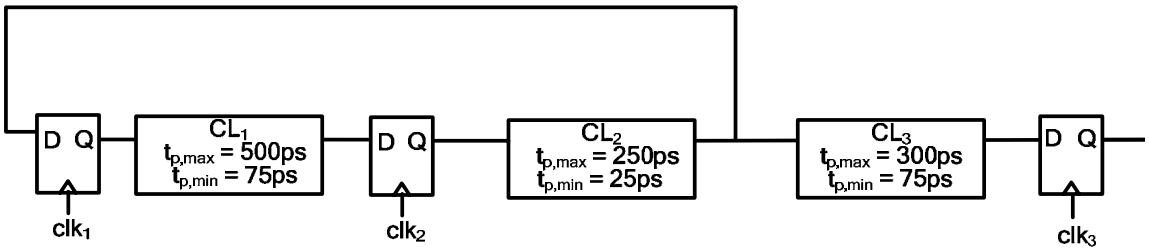


b) **(5 pts)** One of your fellow designers used this latch in their chip, and complains to you that their chip does not function correctly when they make the clock frequency too low. Could this latch design be the cause of the problem? If so, can you add some additional circuitry to the latch to fix this issue?

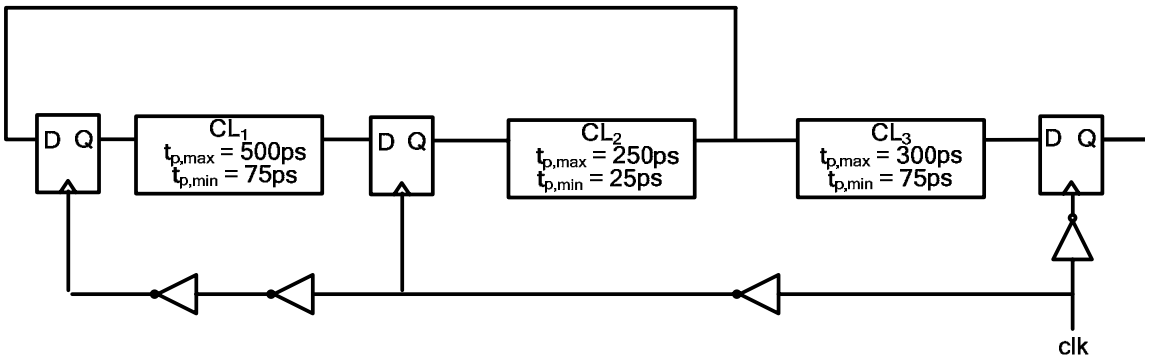
c) **(6 pts)** Your fellow designer has also identified that on this same chip, the latch can fail when the load capacitance it drives is too small. Other than increasing the load capacitance, changing the sizes of the transistors, or applying any fixes that you may have made in part (b), is there any way you can modify the latch in order to eliminate this issue?

PROBLEM 4: Timing and Clock Distribution (26 points)

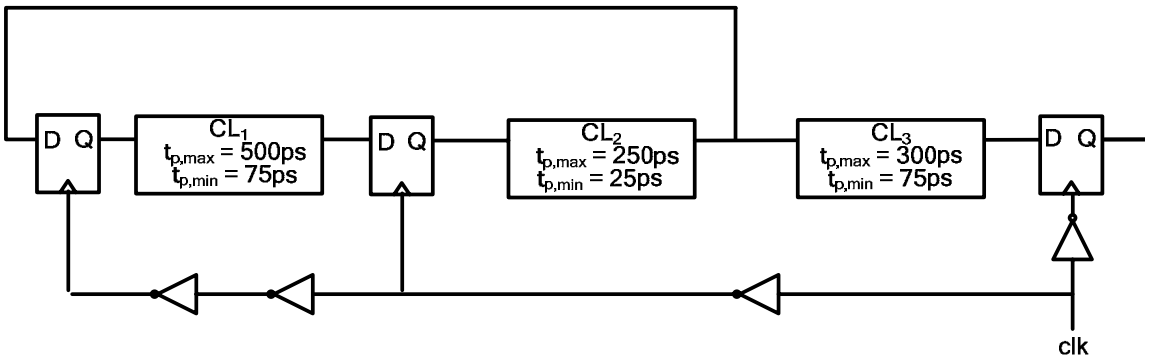
In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figure, and the flip-flops have the following properties: $t_{clk\text{-}q}$ = 50ps, t_{setup} = 50ps, and t_{hold} = 50ps. You can assume that the clock has no jitter.



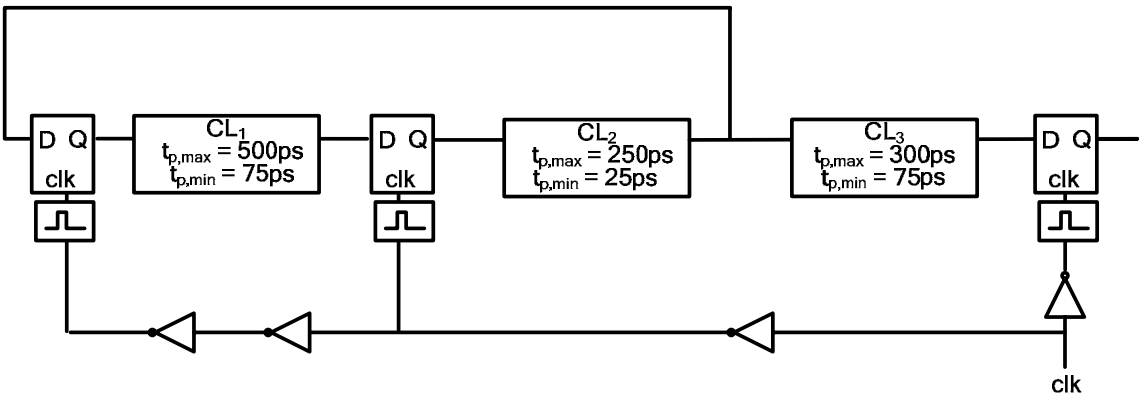
a) (5 pts) Assuming there is no skew between clk_1, clk_2, and clk_3, what is the minimum clock cycle time for this pipeline? Are there any minimum delay (hold time) violations?



b) (5 pts) Now we'll include the clock distribution network for this pipeline. Assuming that the delay of each inverter is nominally 50ps, but that each inverter's delay varies randomly by +/-10%, now what is the minimum clock cycle time?



c) (6 pts) Under these same conditions (i.e., 50ps nominal inverter delay, +/-10% delay variation) this pipeline has a minimum delay (hold time) failure. Can you intentionally add delay into the circuit in order to fix this hold time violation without affecting the minimum clock cycle? Note that you can not modify the clock network – in other words, you can only add delay onto the logic paths.
If this is possible, you should indicate where in the pipeline you want to add delay and calculate how much delay is necessary. If not, you should explain why it isn't possible to eliminate the hold time violation without affecting the minimum cycle time.



d) (10 pts) If we now replace the flip flops by pulsed latches with a pulse width of t_w = 25ps, the same $t_{clk\text{-}q}$, t_{setup}, and t_{hold} as the flip-flops, and with $t_{d\text{-}q} = t_{clk\text{-}q} + t_{setup}$, what is the new minimum cycle time of the pipeline? Can this cycle time be achieved without failing any hold time constraints? Note that you still have the option to add delay like in part (c) in order to fix hold time violations.

PROBLEM 5: Arithmetic (21 pts)

In this problem we will design a circuit that detects the location of the first "1" in a binary input signal. "First" is defined relative to the MSB, and all outputs from the circuit should be zero except for the position where the first "1" occurred. For example, if the input to the circuit was "00101011", the output of the circuit should be "00100000". You can assume that both the true and complement versions of the input are available.

a) **(3 pts)** Assuming the input signal is only 2 bits wide, draw a gate-level schematic (i.e., no transistors) showing how you would calculate the 2-bit output $Out_{1:0}$. Each "gate" can be an inverter, NAND2, or NOR2.

b) **(6 pts)** Draw a gate-level schematic indicating how you would implement this circuit for an 8-bit wide input using the minimum number of gates. Assuming that all of the gates have equal delays, how many gate delays are there on the critical path of this circuit?

c) (12 pts) Your colleague Ace says that assuming that the delay of the gates is independent of their fanout, she can reduce the number of gate delays on the critical path of an 8-bit wide leading 1 detector to only 3. Draw a gate-level schematic of an implementation that achieves this delay.
(Hint: Think about how you can use your design from part (a) along with one additional block to implement something similar to a carry look-ahead adder. Don't worry about the logical polarities – you can assume that you have both the true and complement versions of every intermediate signal in addition to the primary inputs.)