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For all problems, you can assume the following transistor parameters:

NMOS:

$V_{Tn} = 0.75V$, $k'_n = 20\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.75V$, $k'_p = 7\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

Bipolar NPN:

$\beta_F = 100$, $V_{BE(on)} = 0.7V$, $V_{BE(sat)} = 0.8V$, $V_{CE(sat)} = 0.1V$

Wiring:

Aluminum: $C_{parallel\text{-}plate} = 0.03\ fF/\mu m^2$; $C_{fringe} = 0.045\ fF/\mu m$, $R_{sheet} = 0.05\ \Omega/o$,

$L_{alum} = 0.4\ pH/\mu m$

Polysilicon: $C_{parallel\text{-}plate} = 0.06\ fF/\mu m^2$; $C_{fringe} = 0.045\ fF/\mu m$, $R_{sheet} = 10\ \Omega/o$

For all problems, you maty assume that the transistor lengths indicated are the effective lengths (L_{eff}) or, equivalently, that LD = 0.

NAME	
	Last First

GRAD/UNDERGRAD	

All questions are worth 15 points.

1	2	3	4	5	6	7	Total

PROBLEM 1: Logic / Arithmetic

Shown in FIG. 1 are two building blocks for an adder.
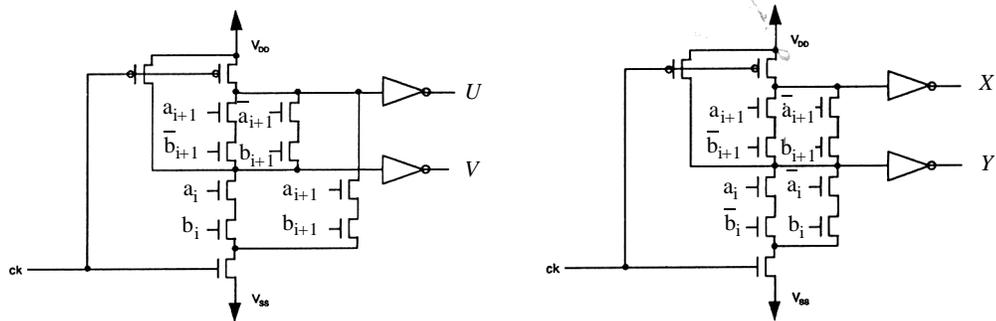
FIG. 1 Buidling blocks

a. Derive the logic function of each of the outputs *U*, *V*, *X*, and *Y*.

U:

V:

X:

Y:

b. What logic style is used for the implementation of this function? Where does it differ from the standard implementation?

c. Would a single PMOS transistor suffice? Why or why not ?

d. Draw a block diagram on how you would connect these modules to create a 16-bit adder.

e. Derive an approximative expression for the worst-case delay of your adder (for N bits).

f. Describe one approach on how these blocks could be used in a better-than-linear adder.

PROBLEM 2: Power Consumption

A capacitor of 20 pF is being charged through a switch with a constant on-resistance of 10 kΩ (FIG. 2a).
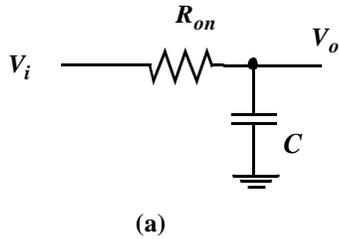
FIG. 2 Switch/capacitor combination
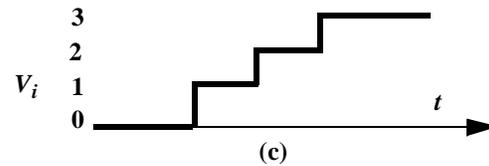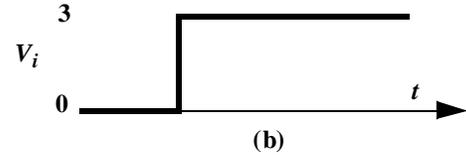
a) A voltage step of 3 V is applied at the input, as shown in FIG. 2b. Compute the energy that is stored on the capacitor when the transaction is completed.

E=

b) Compute the energy dissipated in the switch during the transaction.

E=

c) Instead of applying the 3 V step all at once, the input is applied as a sequence of 1 V steps, as illustrated in FIG. 2c. You may assume that the charge transfer is allowed to complete between the consecutive steps. Determine again the charge stored on the capacator after the complete transaction is finished.

E=

d) Determine the total energy dissipated in the switch during the transaction.

E=

e) Discuss the advantage and disadvantage of this approach. Based on this observations, generalize your findings to come up with a generic technique.

Advantage:

Disadvantage:

Generic Technique:

PROBLEM 3: Sequential Circuits

In this problem, we study a number of "cute" sequential circuits. For each of them, answer the questions posed.

a. Determine the function of the circuit given below. Draw the waveform at the output for a positive and negative going transition at the input In_0. Explain where such a circuit might be useful. Determine an approximative expression for the dominant timing parameter. A dominant timing parameter is for instance the period of an oscillator, the delay of gate, the pulse-width of a monostable, etc.

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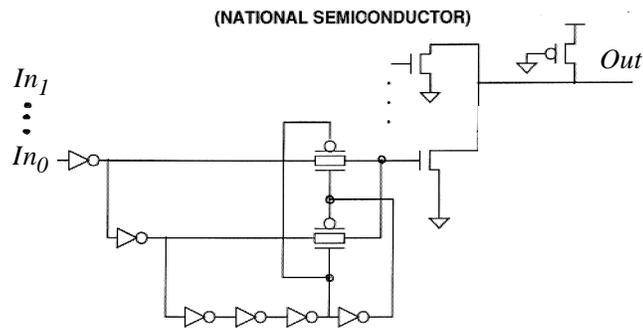
Waveforms

Function of the circuit - where could you use this?

Expression for timing parameter:

b. Determine the function of the circuit given below. Draw the voltage waveforms at nodes X, Y, and Out. Determine again the dominant timing parameter as a function of the circuit parameters. You may ignore the delays of the SR flip-flop and the schmitt trigger.
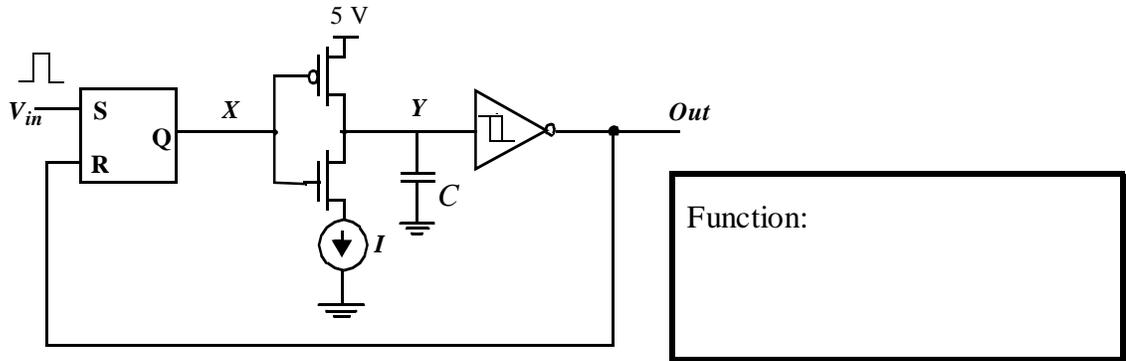
Function:

Waveforms:

Expression:

c. Determine the type of flip-flop given below. Is it edge-triggered, master-slave or a latch? Discuss the function of the inverter and the feedback circuit. Is this circuit sensitive to clock over-lap? Explain?
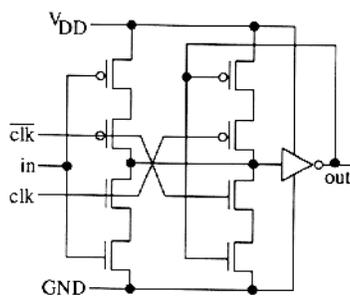
☐ Edge-Triggered Flip-flop

☐ Master-Slave Flip-Flop

☐ Latch

Function of Inverter and Feedback:

Sensitive to Clock Overlap?

PROBLEM 4: Sequential Circuits

A clock driver circuit is given in FIG. 3. Assume that $C_1 = C_2 = C_3 = C_4$, and $C_A = C_B$.
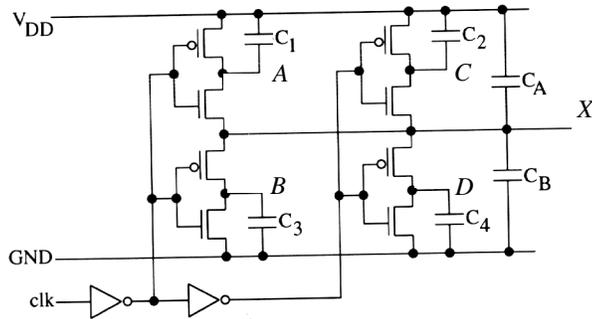
FIG. 3 Clock Driver

a) Write down the equations to determine the voltage at node X for $\phi = 1$ and $\phi = 0$.

b) What will the voltage at that node be in the steady state mode? (Assume that $C_A \gg C_1$)

c) Draw the voltage waveforms at nodes *A*, *B*, *C*, and *D* (in steady state).

d) Discuss the potential usage and advantages of this circuit.

e) All bipolar flip-flops tend to be static. Explain why.

Problem 5: Interconnect

An on-chip CMOS driver has to drive a 10 cm long, 9 μm wide lossless transmission line, implemented on-chip in aluminum. At the destination end, the wire is capacitively terminated. For all practical purposes, we may assume here that this is equivalent to open-ended.
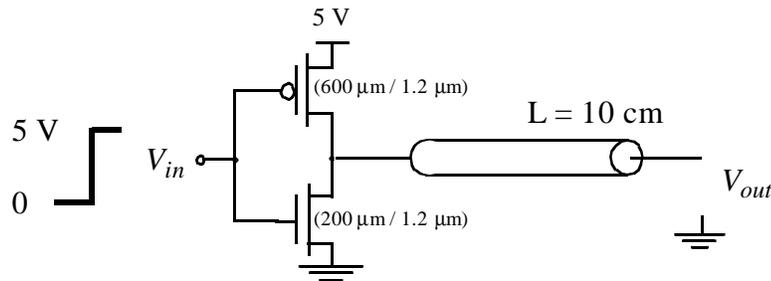
FIG. 4 Driver and Transmission Line.

a. Determine the equivalent on-resistance of the NMOS transistor of the driver (computed for V_{in} between 0 and 2.5 V).

$R_{on}=$

b. Determine the propagation delay of the circuit (for a low-to-high transition at the input). You may assume that the transmission line effect is dominant here. Ignore the parasitic capacitances of the driver.

$t_p=$

c. Size the driver transistors such that this delay is minimized.

$(W/L)_n$

d. Unfortunately, an aluminum wire hardly can be call a "lossless" medium. Determine quantitatively if the resistive or inductive effects dominate for the circuit of FIG. 4.

e. Determine which (single) approach is most effective and practical in CMOS design to combat transmission line effects:

☐ Series termination at the source

☐ Parallel termination at the source

☐ Series termination at the destination

☐ Parallel termination at the destination

Problem 6: Timing

Consider the circuit of FIG. 5. The rectangles represent edge-triggered flip-flops and the circles represent combinational logic. The numbers annotated on the logic blocks represent the minimum and maximum delays of the blocks. For simplicity, all the register and interconnect timing parameters are supposed to be zero. The δ's at the clock inputs of the registers represent the absolute skew between the clock source and the clock port of the register.
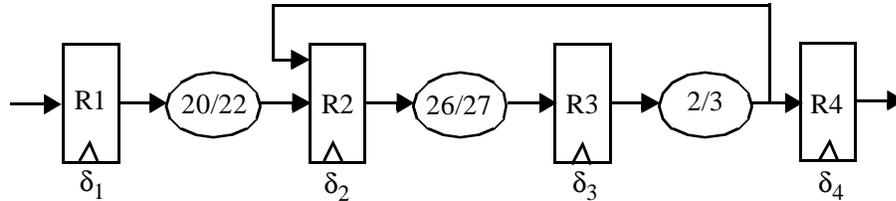
FIG. 5 Sequential circuit.

a. Determine the constraints on the clock skew parameters, so that the circuit does not exhibit race conditions. Hint: you should present four inequalities. DO NOT SOLVE.

Constraints on skew:

b. Derive the constraints that determine the minimum clock period in the presence of skew. Once again, DO NOT SOLVE.

Constraints on clock period:

c. Determine the minimum clock period if no clock skew is present.

┌─────────────────────────────┐
│ **T$_{min}$**   │
└─────────────────────────────┘

d. Determine the minimum clock period if the clock is routed from left to right, i.e. $0 < \delta_1 < \delta_2 < \delta_3 < \delta_4$.

┌─────────────────────────────┐
│ **T$_{min}$**   │
└─────────────────────────────┘

e. Determine the minimum clock period if the clock is routed from right to left, i.e. $\delta_1 > \delta_2 > \delta_3 > \delta_4 > 0$.

┌─────────────────────────────┐
│ **T$_{min}$**   │
└─────────────────────────────┘

Problem 7: Memory

Consider the memory cell given below. The dimensions of the dominant elements of the cell are annotated on the Figure. You may ignore the parasitics introduced by the sections of the design for which no dimensions are given. The polysilicon plate is connected to a 5 V dc supply voltage. The following parameters hold: $C_{ox} = 1.75$ fF/μm^2; $C_{diff}(0) = 3 \times 10^{-4}$ F/m^2; $C_{diffsw}(0) = 0$ F/m. You may assume that junctions are abrupt. $C_{OVERLAP} = 0.25$ fF/μm.
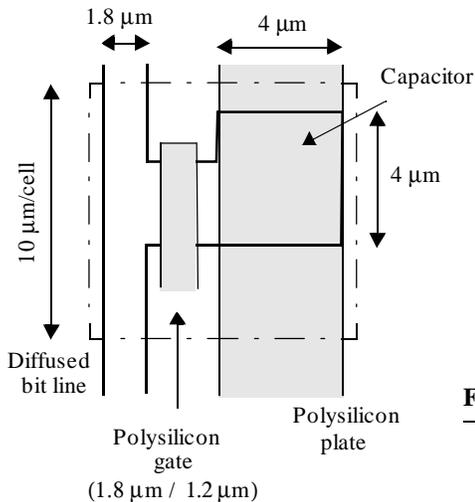
FIG. 6 Memory cell

a. Determine the charge stored on the cell capacitor when a "1" is written into the cell (a 5 V signal is applied to the bit-line. The wordline is switched to 5 V as well).

Q=

b. Determine the charge stored on the cell capacitor when a "0" is written into the cell (a 0 V signal is applied to the bit-line).

Q=

c. Before performing a read operation, the bitline is precharged to 5 V. Determine the capacitance of the bitline at that voltage. You may assume that 256 cells are connected to a single bitline.

$C_{bit}=$

d. Determine the voltage appearing on the bit-line, when reading a "1". The same, when reading a "0".

$V_1=$

$V_0=$

e. Assuming that the access transistor has a constant resistance of 20 kΩ, how long do we have to wait to turn on the sense amplifier after the wordline has been enabled for a read-operation. It is assumed that the sense amplifier is turned on after the bitline voltage has reached 90% of its final value.

$t_{delay}=$