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EECS 141: FALL 95—MIDTERM 1

For all problems, you can assume the following transistor parameters:

NMOS:

$V_{Tn} = 0.75V$, $k'_n = 20\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.75V$, $k'_p = 7\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

For all problems, you maty assume that the transistor lengths indicated are the effective lengths (L_{eff}) or, equivalently, that $LD = 0$.

NAME	Last First

GRAD/UNDERGRAD	

Problem 1:

Problem 2:

Total	

PROBLEM 1: MOS Inverter

Consider the fictitious gate of Figure 1. The I-V characteristic of the load device L_1 is given in the Figure as well.

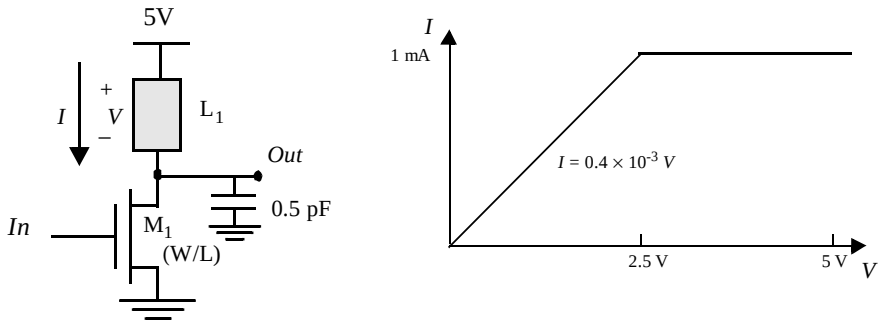

FIG. 1 MOS Inverter

a. Determine $(W/L)_{M1}$ such that a V_{OL} of 1V is obtained.

W/L =

b. Write down the equation(s) you would use to solve for V_{IH}.

Eq. 1: **(Eq. 2:)**

c. Find t_{pHL}.

t_{pHL}=

d. Determine the average static power consumption, assuming that the input is high 75% of the time.

P_{stat} =

f. Figure 2 shows the load-lines of two possible load devices. Determine which one is better (a or b) for each of the following gate properties and explain in ONE line why.

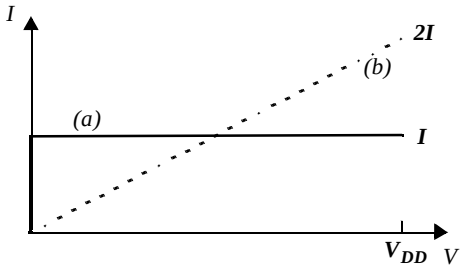

FIG. 2 Load lines of two load devices (a) and (b).

Property	(a) or (b)	Why
V_{OL}		
t_{pLH}		
t_{pHL}		
P_{stat}		

Problem 2: Combinational Logic

The gate below has the advantage of being simple and requiring the minimum number of transistors for the function intended.

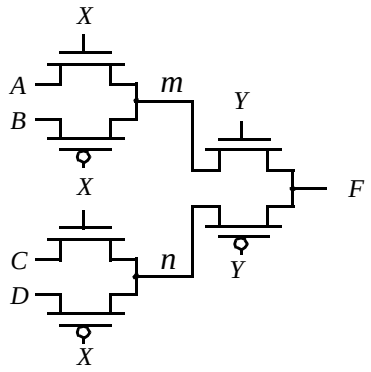

FIG. 3 : Complex Gate

a. Derive the boolean expression for *F*. What logic function does this gate implement?

F =

Logic function:

b. Determine the **exact** output voltage for each of the following conditions (assume that the supply rails — and the logic levels at the inputs — are set at 0 V and 3.3 V):

A = 0; X = 1, Y = 1	V_{out} =
A = 1; X = 1, Y = 1	V_{out} =
B = 0; X = 0, Y = 1	V_{out} =
B = 1; X = 0, Y = 1	V_{out} =
D = 0; X = 0, Y = 0	V_{out} =
D = 1; X = 0, Y = 0	V_{out} =

c. Determine t_{pLH} and t_{pHL} between node B and the output for X = 0 and Y = 1. You may assume an equivalent resistance of 10 kΩ for an NMOS transistor and 25 kΩ for a PMOS. The capacitance at nodes m and n equals 100 fF, while node *F* is loaded with 300 fF.

t_{pLH} =

t_{pHL} =