



University of California
College of Engineering
Department of Electrical Engineering
and Computer Science

Jan M. Rabaey

TuTh 2:00-3:30 pm

Andrei Vladimirescu

ee141@bwrc

EECS 141: SPRING 02 – MIDTERM 2

PROBLEM 1: Logic Design

For the gate shown below assume that

- each NMOS drain or source contributes 1 fF from the node it is connected to ground;
- each PMOS drain or source contributes 3fF from the node it is connected to ground;
- the ON resistance of the NMOS equals that of the PMOS and is 10k

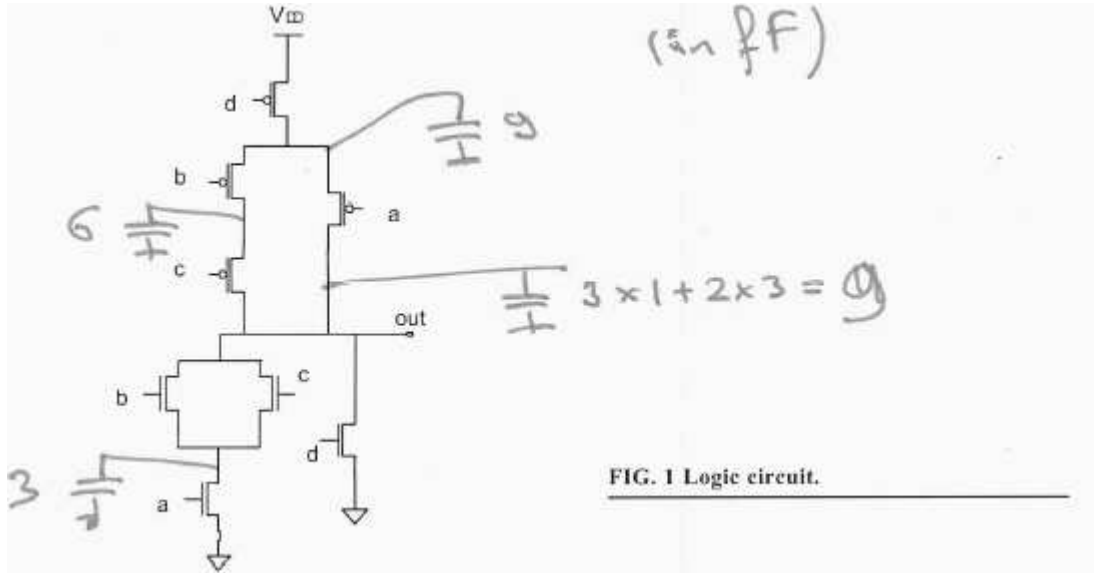
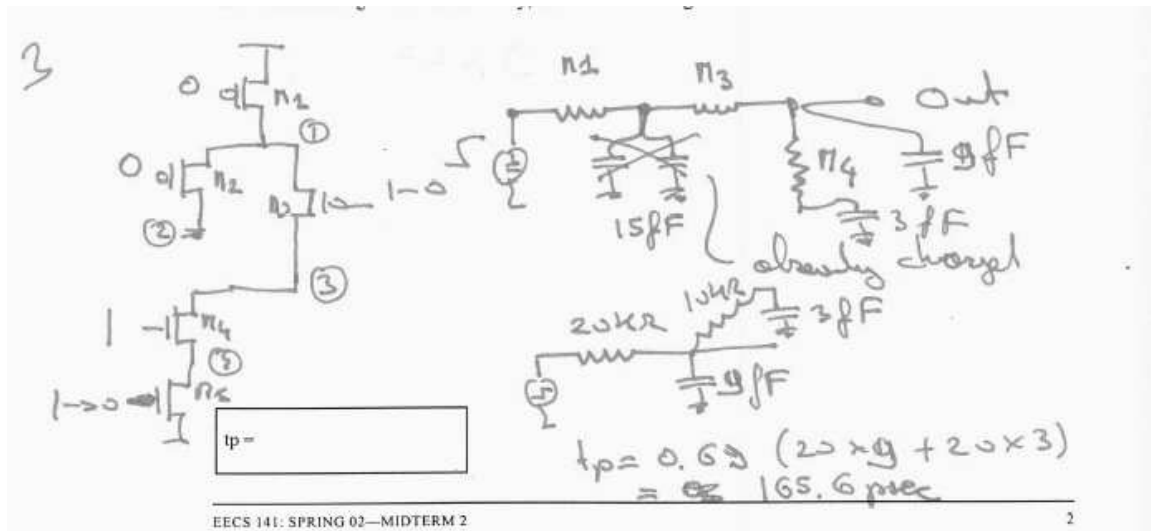


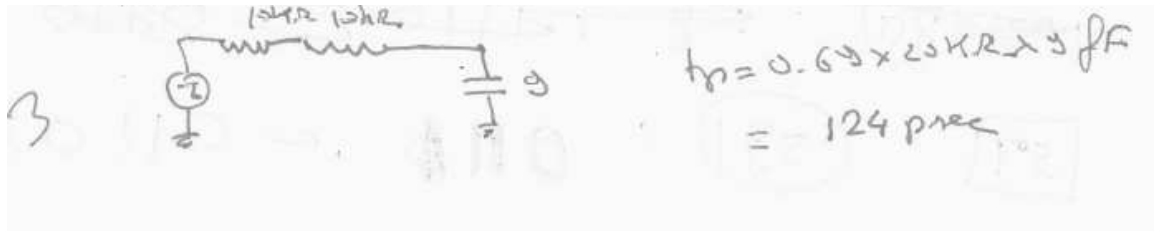
FIG. 1 Logic circuit.

- a) Attach the capacitance at each node in the diagram (rejoice: this is a freebie).
- b) Find the Ellmore delay when the inputs abcd are initially 1010 and then a switches 1->0. Make sure to draw the equivalent circuit diagram you are using.

Hint: "if an intermediate capacitance is already precharged to the correct value, assume that this capacitor contributes nothing to the Ellmore delay, and can hence be ignored in the model."



c) Find the Ellmore delay when the inputs abcd are 1000 and then c switches 0->1



$t_p = 124 psec$

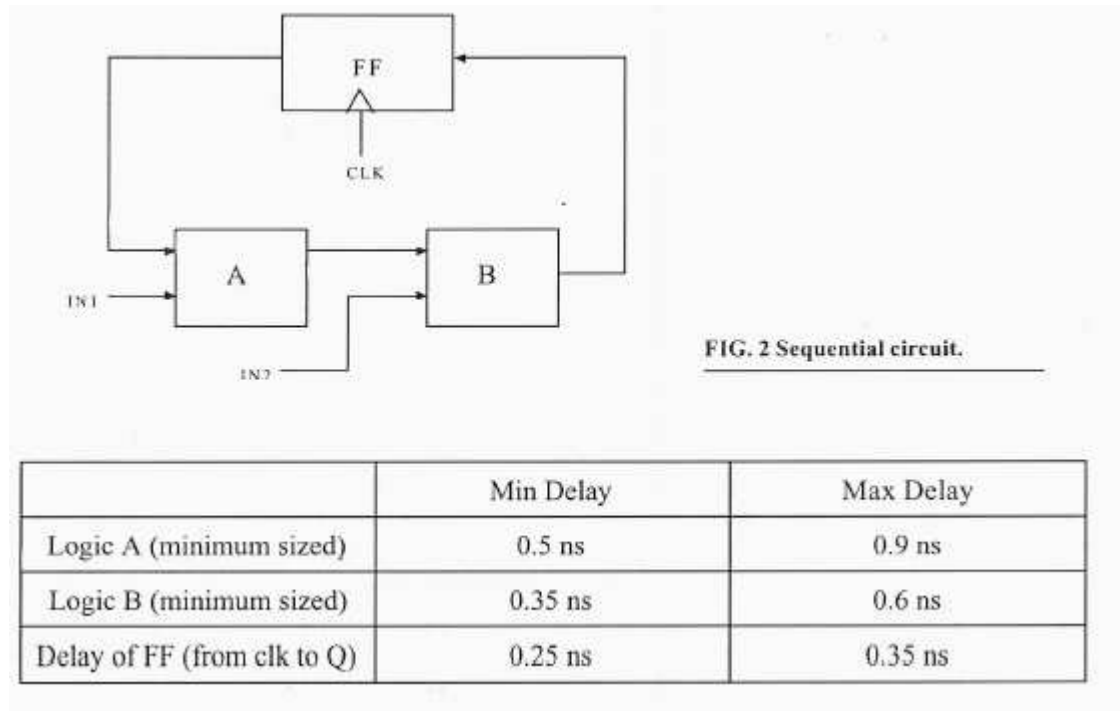
d) Find the initial condition, and the input that needs to switch **for a minimum delay**.
 NOTE: Only **one** input is allowed to change

switch output low & through it, & minimize capacitance -

0110 → 0111

PROBLEM 2: Sequential Circuits

Consider the logic circuit given below. The FF used is positive-edge triggered. The timing parameters for logic gates and flip-flops are shown below.



Setup time for FF = 0.15 ns

Hold time for FF = 0.55 ns

The logic in block A and block B can each be sized up by a factor. You may assume that both the min and max delays decrease linearly with increasing size. For example, if logic B were increased by a factor of 2, the minimum delay would be 0.175 ns and the maximum delay would be 0.3 ns.

- a) Assuming that logic block B is kept at minimum size, how large would block A have to be for the sequential circuit to work correctly if the block were to run at 800 MHz?

critical path: $T \geq t_{FF, \max} + \frac{t_{A, \max}}{S_A} + t_{B, \max} + t_{\text{setup}, \max}$

$T = 1.25 \text{ nsec} = 1/800 \text{ nsec}$

$1.25 \text{ nsec} \geq 0.35 \text{ nsec} + \frac{0.9}{S_A} + 0.6 + 0.15$

size A = 6 $\Rightarrow S_A = 6$

- b) We would like to keep this circuit as small as possible. Hence, we decided to keep block A at 2 times minimum size. Determine the fastest possible clock speed we can run this circuit at, if we are free to size block B. Explain your answer.

Maximum performance based on critical path.

$$T \geq t_{FF, \max} + \frac{t_{A, \max}}{2} + \frac{t_{B, \max}}{S_B} + t_{\text{setup}}$$

would be obtained for $S_B = \infty$

But: check hold time

$$t_{\text{hold}} \leq t_{FF, \min} + \frac{t_{A, \min}}{2} + \frac{t_{B, \min}}{S_B}$$

$$f_{\max} = 965.52 \text{ MHz}$$

$$0.55 \leq 0.25 + \frac{0.5}{2} + \frac{0.35_{\min}}{S_B}$$

Is violated for $S_B = 7$

$$T_{\min} = 0.35 + \frac{t_A}{2} + \frac{t_B}{7} + 0.15 = 0.35 + 0.15 + \frac{0.9}{2} + \frac{0.6}{7}$$

$$= 1.036 \text{ nsec}$$

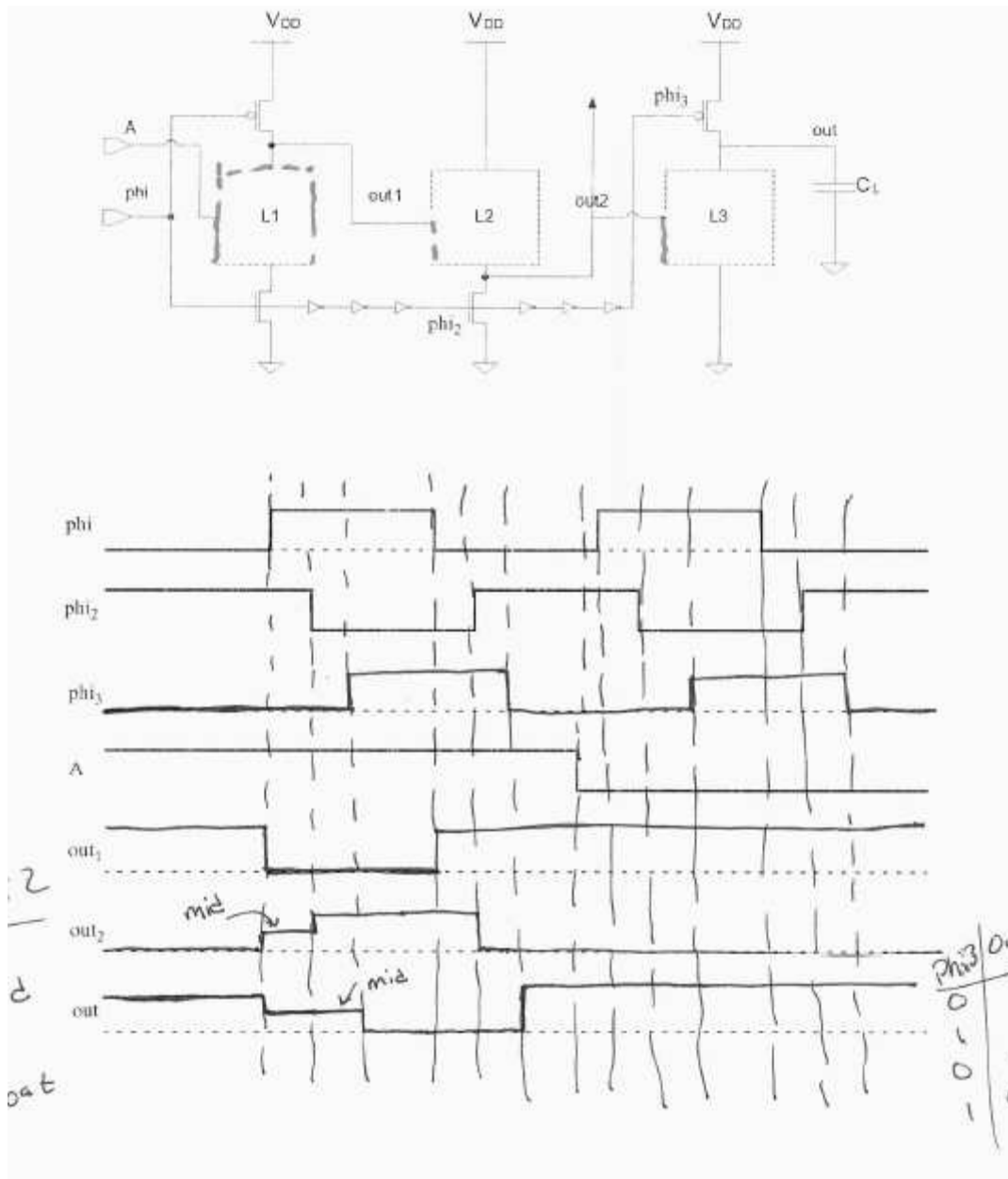
$$\text{or } f_{\max} = 965.52 \text{ MHz}$$

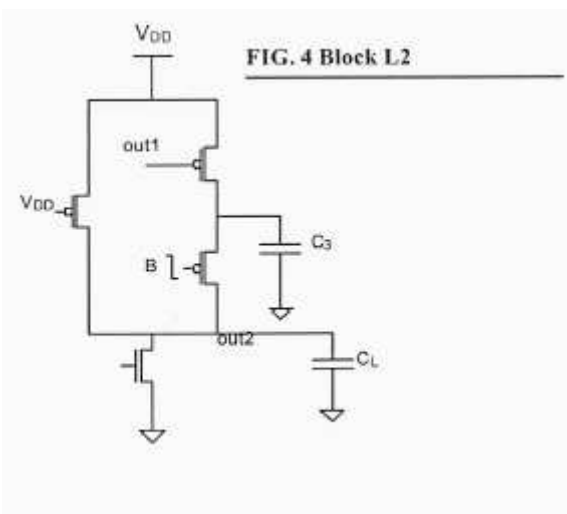
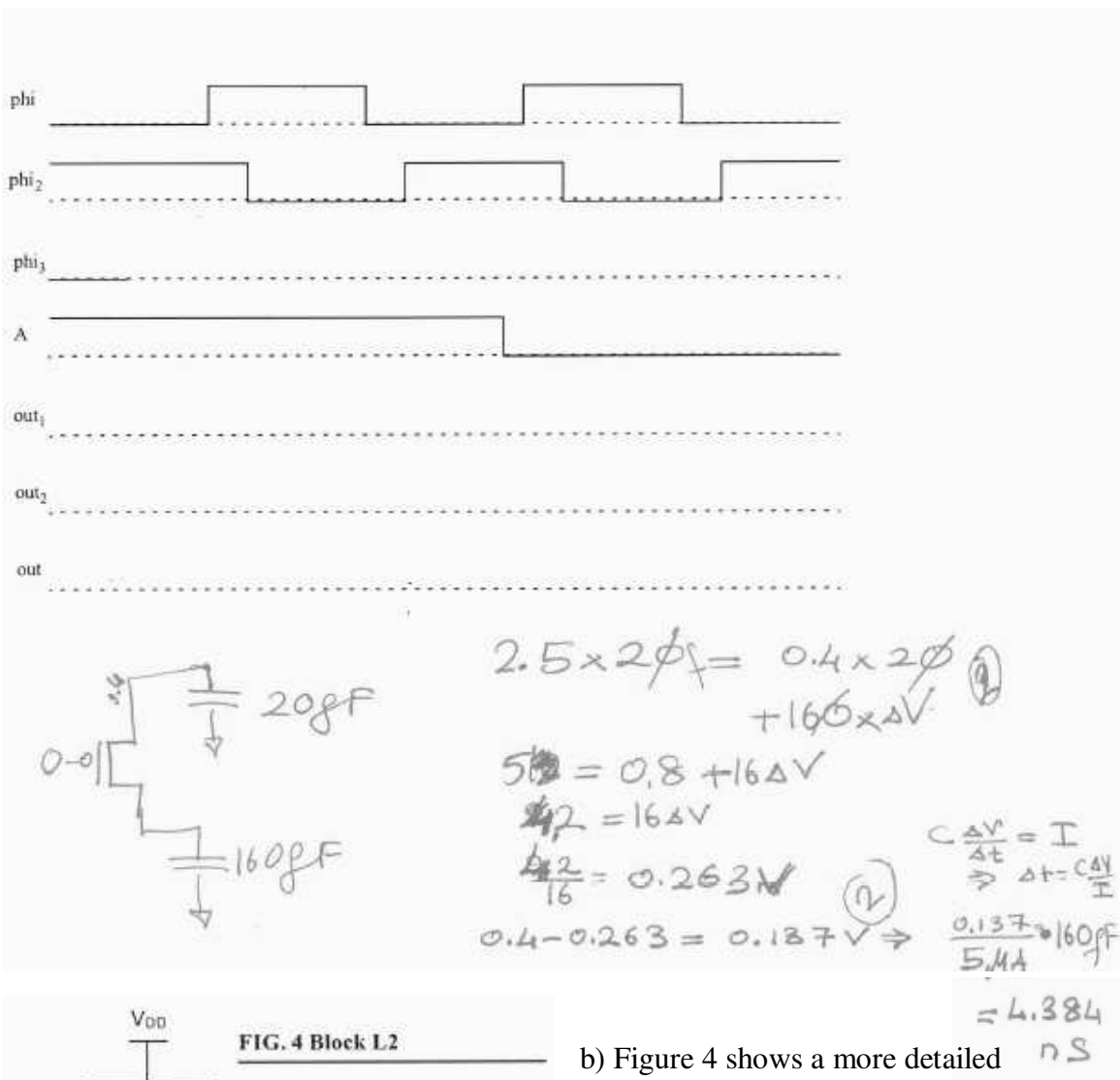
PROBLEM 3: Dynamic Logic

a. Yet another one of those brilliant designs. Designer Jane Doe figured out how to reduce the number of transistors in a dynamic block, and hence get a better performance by using the concept of staggered clocks (something she heard about on the grapevine).

You may assume the following design parameters: $V_{dd} = 2.5V$. $V_{Tn} = V_{Tp} = 0.4V$.

- Assuming that each gate (L1, L2, and L3) implements an inverter, fill in the waveforms for nodes ϕ_3 , out1, out2, and out, on the diagram below. Assume that each inverter in the block chain has a fixed delay of 100 psec, and so does each of the dynamic logic blocks.





b) Figure 4 shows a more detailed schematic of block L2 of the logic module of Figure 3. We are given that $C_L = 160 \text{ fF}$ and $C_3 = 20 \text{ fF}$. Also, due to the high temperature of the chip, it turns out that there is a net leakage current of $5 \mu\text{A}$ flowing **into** node “out2” when it is low. Input B switches soon after the evaluation begins. Determine the maximum length of the evaluation period so that proper operation of this block and the following block (L3) is ensured (**assume the worst-case conditions**).