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EECS 141: SPRING 97 —MIDTERM 1

For all problems, you can assume the following transistor parameters:

NMOS:

$V_{Tn} = 0.75V$, $k'_n = 20\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.75V$, $k'_p = 7\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

NAME	Last First

GRAD/UNDERGRAD	

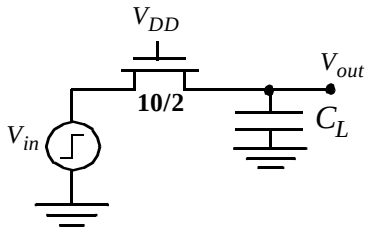
Problem 1:

Problem 2:

Total	

Problem 1: Static and dynamic analysis

Consider the following logic circuit:



a. Assume that $V_{out}(t = 0) = 0$ V. Determine V_{out} (t = ∞) when V_{in} is raised from 0 V to V_{DD} at $t = 0$. Assume $V_{DD} = 3$ V. You may assume that $L = L_{eff}$, or that the lateral diffusion can be ignored in this problem.

V_{out}(t=∞):

b. Determine t_{pLH} at V_{out}. Assume an ideal step at the input. The external load capacitance C_L can be assumed to be large and equals 10 pF.

t_{pLH} =

c. Determine the energy that is stored on C_L at the end of the low-to-high transition. How much energy was dissipated in the MOS transistor? How much was delivered by the input source? **HINT: Derive the results; Do not take the equations in the book for granted!**

$E(C_L)$ =
$E(MOS)$ =
$E(V_{in})$ =

d. Assume that the NMOS is replaced by a PMOS device of the same size with its gate connected to GND. Determine the impact on the following design parameters, and give a short explanation

	EXPLAIN:
V_{out} **(t = ∞):** ☐ Larger ☐ Equal ☐ Smaller	
t_{pLH}**:** ☐ Larger ☐ Equal ☐ Smaller	
$E(V_{in})$**:** ☐ Larger ☐ Equal ☐ Smaller	

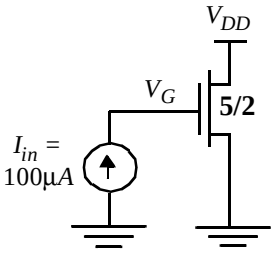
e. Describe in a couple of sentences how you would decrease the delay of this gate. Is there an absolute lower limit on the delay, and if yes explain why and give an approximate value of this delay.:

How would you reduce the delay?

Absolute minimum delay? Why?

Approximate value of minimum delay

PROBLEM 2: MOS Capacitances



Consider the following simple circuit (implemented in the 1.2 μm CMOS technology). Assume V_{DD} = 3 V and use the following transistor parameters: C_{ox}= 1.75 fF/μm^2, x_j (lateral diffusion) = 0.15 μm, C_{j0}=3.0×10^{-4} F/m^2, m_j=0.5, C_{jsw}=8.0×10^{-10} F/m, m_{jsw}=0.5.

Assume that V_G is initially at 0 V. We want the compute the time it will take to raise V_G to V_{DD}. To do so, we will lump the device parasitic capacitances into a single lumped capacitance. This capacitance is a function of the operation region of the device.

a. Determine the operation regions the MOS transistor is traversing during the transient (for V_G going from 0 to V_{DD}).

Region 1:

Region 2:

Region 3:

...

b. Determine the (average) lumped capacitance seen at the gate of the MOS transistor in each of these regions.

C_g (region 1):

C_g (region 2):

C_g (region 3):

c Determine the total time it will take for V_G to go from 0 V to V_{DD} (for I_{in}= 100 μA),

t(0'V_{DD}):