Fall 2000

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS143 Final Exam

Family Name ________________________ First name____________________________

Signature____

Make sure your copy of the exam paper has 14 pages (including cover page)

Instructions: DO ALL WORK ON EXAM PAGES
This is a 3-hr exam (10 sheets of notes allowed)

Grading: To obtain full credit, show correct units and algebraic sign in answers.
Numerical answers which are orders of magnitude off will receive no partial credit.

Problem 1 (25 points)________________

Problem 2 (25 points)_______________

Problem 3 (15 points) ________________

Problem 4 (15 points) ________________

Problem 5 (20 points) ________________

Problem 6 (25 points) ________________

Problem 7 (25 points) ________________

TOTAL (150 points) ___________________

Information which may be useful

$\varepsilon_s = 1.036 \times 10^{-12}$ F/cm for Si

$q = 1.6 \times 10^{-19}$ coulombs

Boltzmann constant $k = 8.62 \times 10^{-5}$ eV/K

$\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm for SiO_2

n_i of Si $= 1.45 \times 10^{10}$ cm^{-3} at 300K

E_g of Si = 1.10 eV at 300K

Electron Affinity of Si = 4.15 eV

Electric potential $\phi = (E_f - E_i)/q$

$n = n_i \exp(q\phi/kT)$

$$x_d = \left[\frac{2\varepsilon_s}{q} (\phi_i - V_a) \left(\frac{1}{N_a} + \frac{1}{N_d}\right) \right]^{1/2}$$

MOS: $V_{GB} = \phi_{MS} + V_{ox} + V_{Si}$

$$V_{FB} = \phi_{MS} - \frac{1}{C_{ox}} \left[Q_f + \int_0^{x_{ox}} \frac{x\,\rho_{ox}(x)}{x_{ox}} dx \right]$$

MOSFET (n-channel):

$$I_{DS} = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_T) V_{DS} - V_{DS}^2/2 \right]$$ (below saturation)

$$I_{Dsat} = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_T)^2/2 \right]$$ (above saturation)

Problem 1 Lab Questions (25 points total)

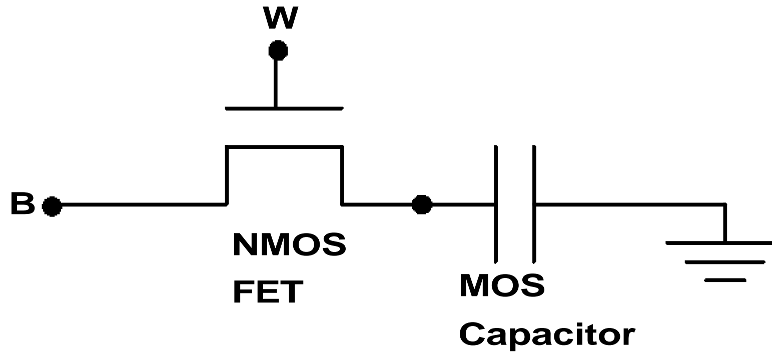
(a) (10 points) We use positive photoresist in the EE143 lab. The fabricated device dimensions are different from the mask dimensions. State qualitatively (increase =↑, decrease = ↓, none = 0) the effect of the following steps on the channel length L and channel width W of the MOSFETs.

	L	W
Increased field oxide thickness		
Longer source/drain drive-in time		
Overdeveloped gate photoresist		
Overdeveloped contact hole photoresist		
Overdeveloped metal photoresist		

(b) The simple circuit shown below is a dynamic random access memory (DRAM) cell. It consists of one MOSFET and one MOS capacitor. You have to design a process flow with the available processing facilities in **CORY 218** only !

Constraints:

Poly-Si , ion implantation, CVD oxide and CVD nitride **will NOT** be allowed in your process flow.



(i) (5 points) Can you make self-aligned source and drain structure in your process with the above limitations? Explain why or why not.

Problem 1 Lab Questions part (b) continued

(ii) (10 points) Design a process flow for your proposed process. Draw the cross-sections of your structure which shows all the salient features of the circuit after each masking step. Label all layers. Your design has to use the minimum number of masking steps.

Problem 2 General Questions (25 points total)

(a) (6 points) Discuss how the Short Channel Effect of MOSFETs (i.e., V_T **decreases** when channel length L decreases) be affected by :

(i) Increasing the substrate doping concentration

(ii) Decreasing the gate oxide thickness.

(b) (7 points) The following schematic shows the enhanced pressure at corners of protruded structures during CMP (Chemical-Mechanical polishing)

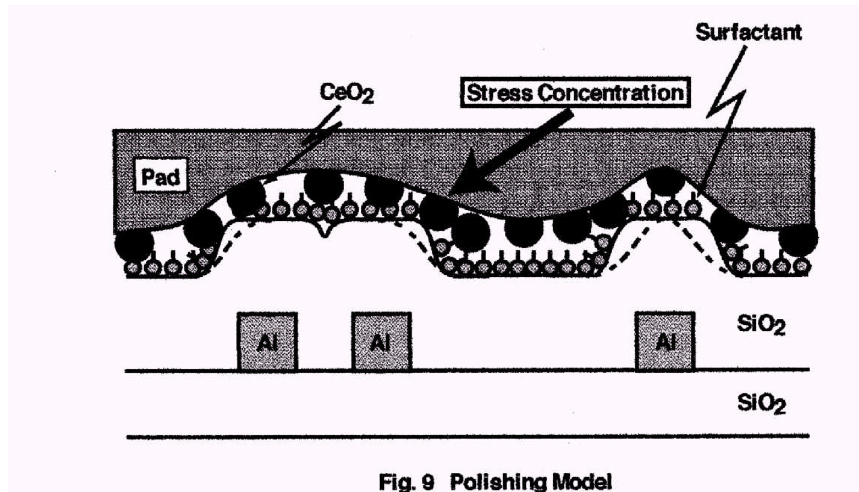


Fig. 9 Polishing Model

Use the Preston equation Use the Preston's Equation: $dH/dt = K \bullet p \bullet v$

where dH/dt = local thickness removal rate

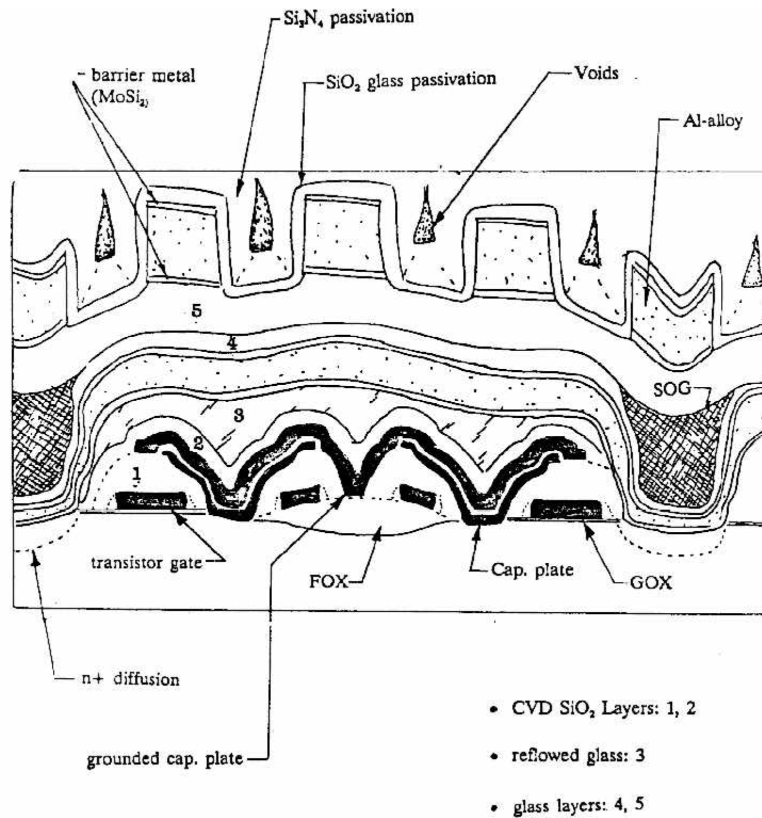
p = local normal force between pad and surface

v = local relative pad-surface velocity

to explain how planarization is achieved by CMP.

Problem 2 continued

With reverse engineering, you uncovered the cross-section of the following MOS integrated circuit product:



(i)(4 points) What is the purpose of using pockets of SOG (spin-on-glass) ?

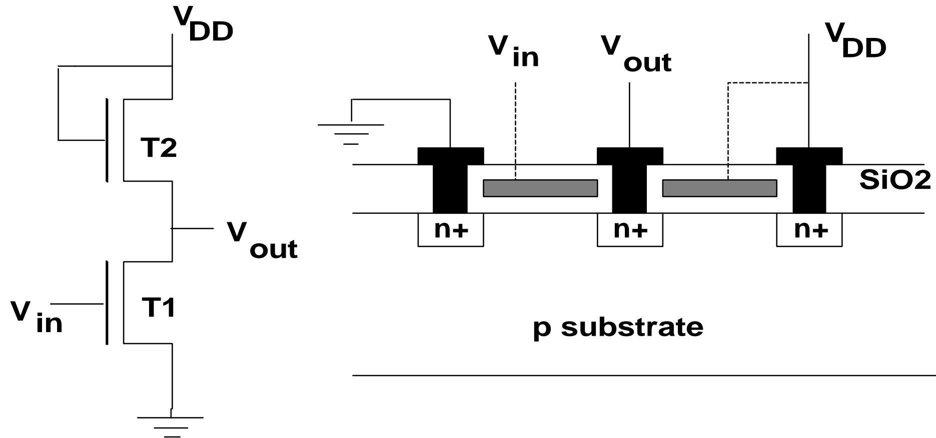
(ii)(4 points) Which deposition method is used for the Si_3N_4 passivating layer ?Why are voids formed?

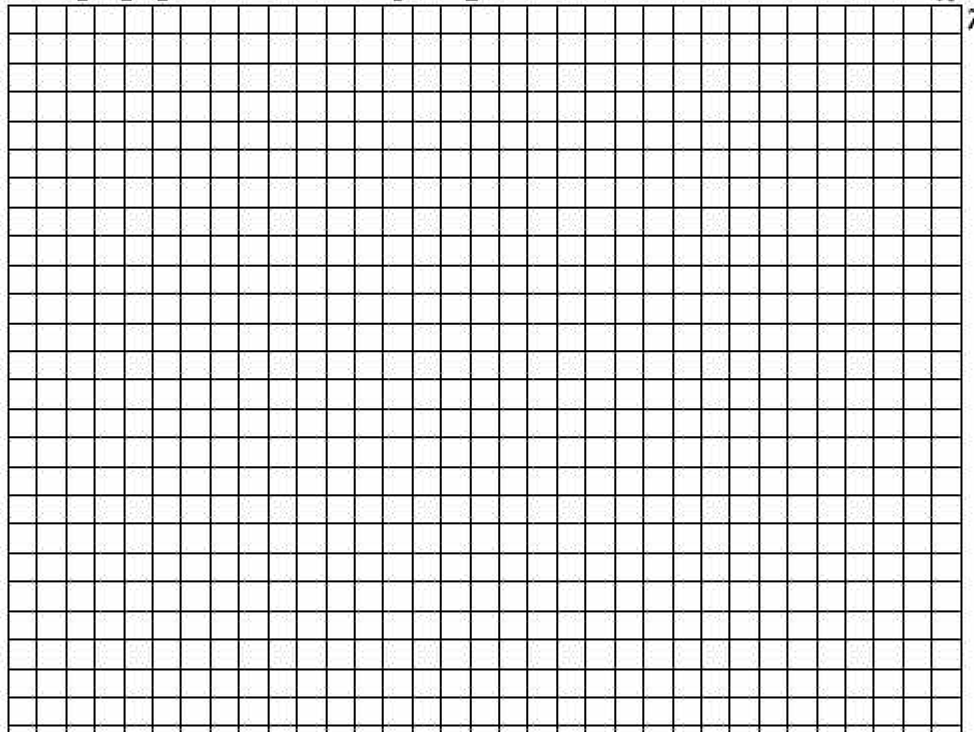
(iii)(4 points) Instead of LOCOS, what oxide isolation scheme will you propose to improve planarization. Illustrate with a sketch.

(iv)(4 points) Which deposition method is used to form the contact and interconnect metalization $MoSi_2$/Al alloy/$MoSi_2$ sandwich ? Suggest an alternative metallization scheme to improve planarization.

Problem 3 Layout (15 points total)

Layout a minimum geometry NMOS (poly-gate) inverter. The poly-gate of the load transistor is connected to its drain with **aluminum** lines.





List of design rules used :

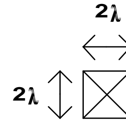
Reference for Problem 3 on Layout : EE143 Standard Layout symbols and Design Rules

1. Background

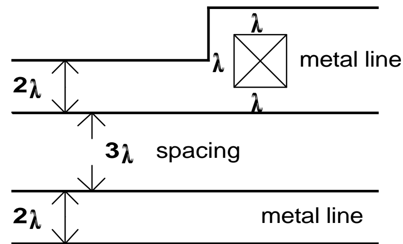
1.1 Lithography/etching limit on minimum feature or spacing = 2λ
1.2 Alignment limit (overlay accuracy) = λ
1.3 Unless specified, default value: λ = 2 μm

2. Symbols and Rules

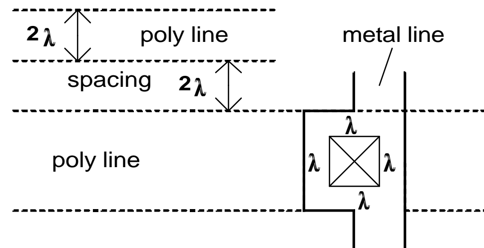
2.1 Contacts (metal to silicon)
minimum size 2λ x 2λ



2.2 Metal
minimum width: 2λ
minimum spacing: 3λ
minimum underlap of contact: λ



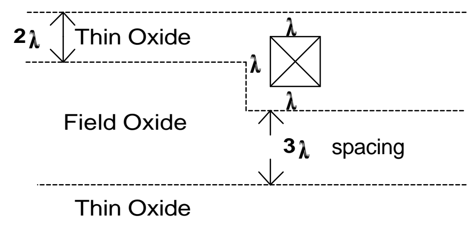
2.3 Polysilicon
minimum width: 2λ
minimum spacing: 2λ
minimum underlap of contact: λ



3. MOS Devices

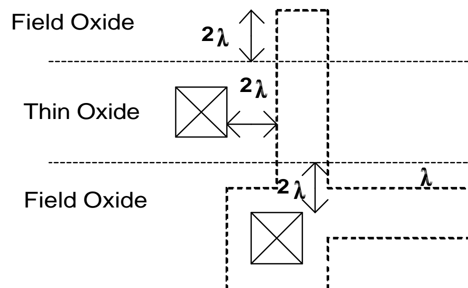
3.1 Thin oxide of MOS
minimum width: 2λ
minimum space: 3λ
minimum underlap of contact: λ

[The thin oxide region is also known as diffusion region. The field oxide region is also called the thick oxide region]



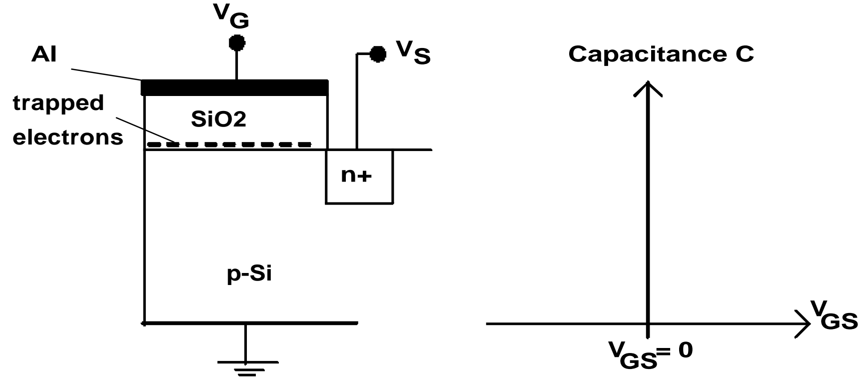
3.2 Si Gate of MOS

Minimum gate overlap of field =2λ
Minimum contact to gate spacing =2λ
Contacts to polysilicon allowed on thick oxide only. Minimum spacing to thin oxide = 2λ
Minimum poly to thin oxide spacing = λ

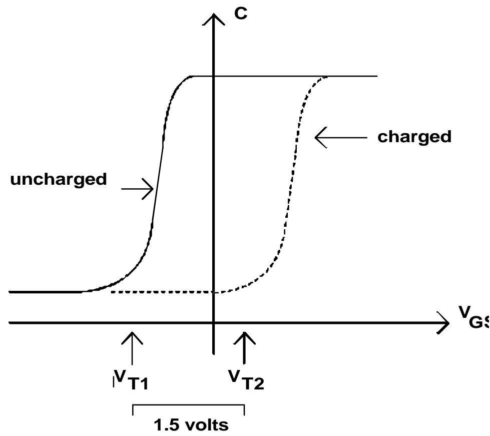


Problem 4 Threshold Voltage Calculation (15 points total)

The following Aluminum-gate two-terminal device structure can be used for semiconductor memories. Suppose we have a way to inject **electrons** in the oxide just at the Si-SiO_2 interface so that they become fixed interface charges. We can then measure the small-signal capacitance, C , of the structure across the G and S terminals.



The C versus V_{GS} curves for **both** the uncharged and charged states are sketched below. Without inversion, the n+ contact is not electrically connected with the channel and the capacitance between G and S is just some small fringing capacitance between the n+ contact and the channel depletion charges In the inversion mode, capacitance becomes C_{ox}. A large C can be interpreted as the charged state (i.e., with the trapped electrons) and a small C can be interpreted as the uncharged state (i.e., without the trapped electrons). [



(a) (10 points) We would like to have a voltage sensing window of 1.5 volts to separate the charge and uncharged states. What is the **minimum** amount of negative charge (i.e., the trapped electrons) that needs to be stored at the Si-SiO_2 interface to make this possible ?

Given: $q\phi_M$ of Al = 4.1 eV , SiO_2 thickness = 500 Å , Substrate doping concentration N_a= $10^{15}/cm^3$

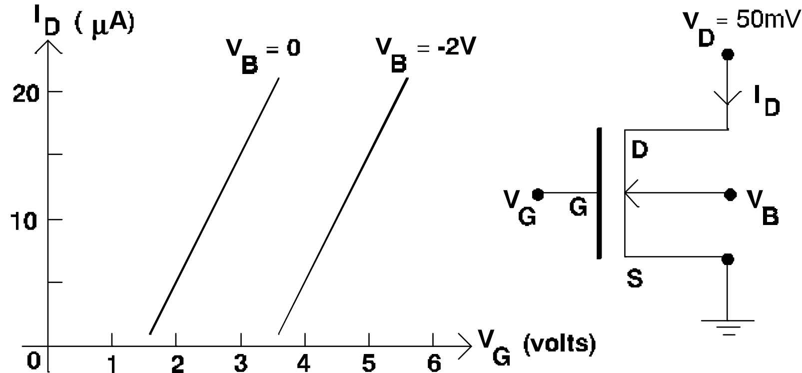
Initial interface charge Q_f without electron trapping =0

Problem 4 continued

(b) (5 points) Using the minimum trapped electron charge in part (a) , we would like to choose a gate voltage halfway between V_{T1} and V_{T2} (the charged and uncharged threshold voltages) as the ideal sensing voltage. What is the value of this gate voltage?

Problem 5 MOS I-V (20 points total)

The I_D versus V_G curves for a n-channel enhancement-mode MOSFET with a fixed V_{DS} (=50 mV) are shown below. The transistor channel length is 10 μm and the channel width is 100 μm, with a gate oxide thickness of 1000 Å.



(a)(5 points) Find the threshold voltages for (i) V_B=0 and (ii) V_B=-2V.

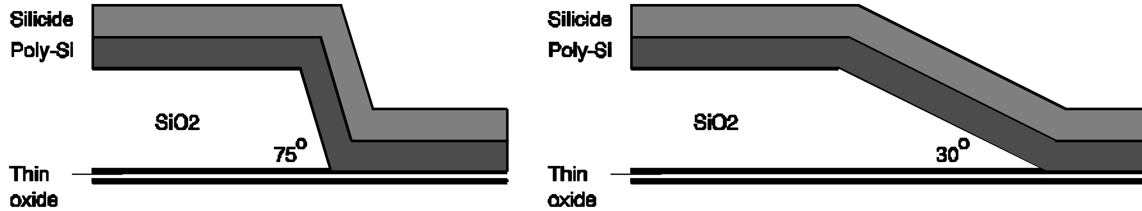
(b)(5 points) Find the substrate doping concentration (assume the substrate is uniformly doped).

(c)(5 points) Find the carrier mobility in the channel.

(d)(5 points) Find I_{Dsat} of the transistor for V_B=0 and V_G =10V .

Problem 6 Reactive Ion Etching (25 points total)

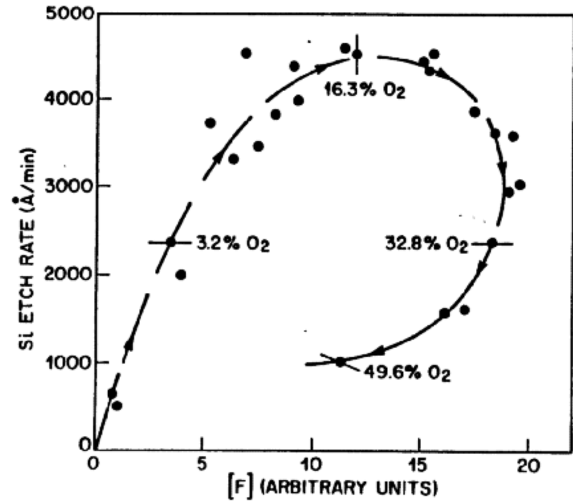
(a)Selectivity (15 points)
The following cross-sections show equal thickness of silicide and polysilicon over SiO_2 steps. A particular anisotropic RIE process has a 2:1 etch rate ratio for silicide to polysilicon.



Assume SiO_2 is not attacked by the RIE process, sketch the cross-sections for both cases:
(i) when the polysilicon is just exposed

(ii) when the thin-oxide is just exposed

(b) (10 points) The Si etching rate in a CF_4/O_2 plasma is plotted as a function of F-atom concentration for various oxygen content. Explain (i) why the etching rate increases with [F] when oxygen content is lower than 16% and (ii) why the rate drops with further increase of oxygen content, and the corresponding decrease of [F].

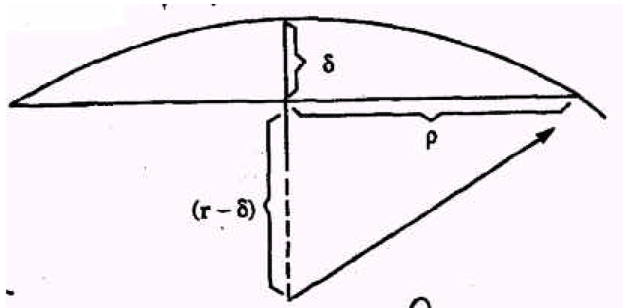


Problem 7 MEMS (25 points)

The stress of thin films on thick wafer substrates can be determined from the amount of bow of the substrate.

$$\sigma_f = \left(\frac{\delta}{3\rho^2}\right)\left(\frac{Y}{1-\nu}\right)_s \frac{t_s^2}{t_f}$$

where δ = maximum bow height and ρ = wafer radius.

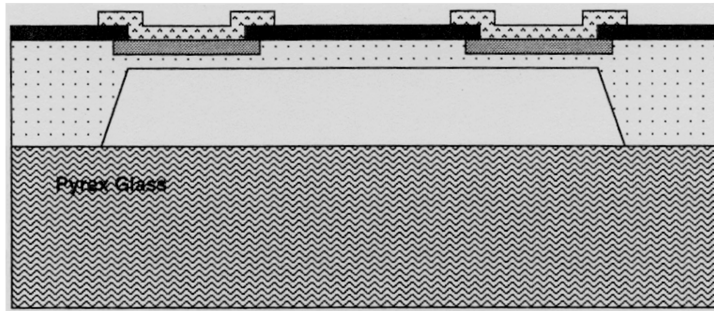


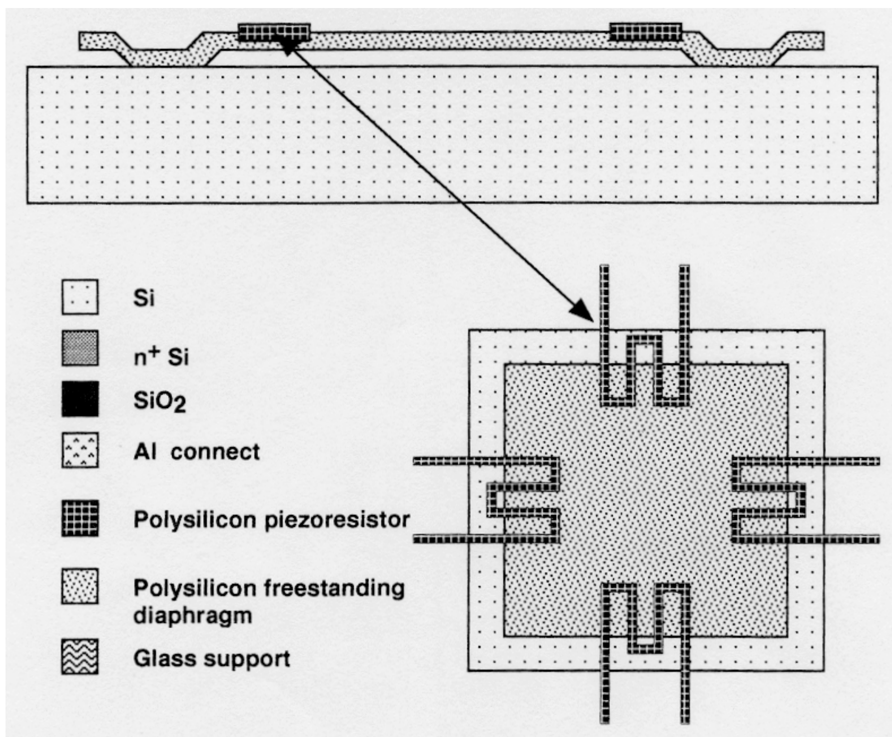
(i) (6 points) Given a wafer radius of 10 cm and a bow of 10,000Å calculate the **stress** for an unknown film 1 µm thick. The substrate is a 400 µm thick Si wafer (assume $Y/(1 - \nu)$ for Si = 1.8×10^{11} N/m^2). Is the thin-film stress tensile or compressive ?

(ii) (4 points) If the thin film in part(a) has a smaller coefficient of thermal expansion than Si. Will you expect δ will increase or decrease when measured at elevated temperartures? Explain briefly.

Problem 7 continued

(b) (15 points) Design a process flow to fabricate the following piezoresistance transducer. Show cross-sections at major processing steps.





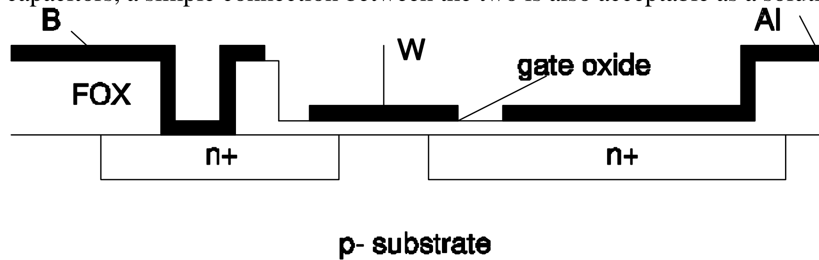
Problem 7 continued (blank page)

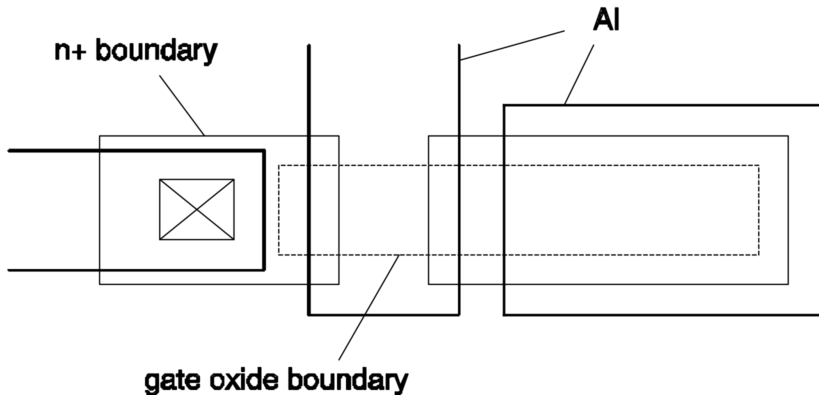
EE143Fall 2000 Final Exam Sample Solutions
Problem 1 Lab Questions
(a)

	L	W
field oxide	0	↑
source/drain drive-in	↓	0
overdeveloped gate photoresist (positive)	↓	↓
overdeveloped contact hole photoresist (positive)	0	0
overdeveloped metal photoresist (positive)	0	0

(b)
(i) Since we have to use aluminum gate and no CVD oxide or nitride is allowed, we cannot use the self-aligned process because Al is deposited after the S/D high-temperature diffusion step. [The dummy gate idea will not work because we have no CVD oxide process]. The MOS structure will have to allow the Al to overlap the n+ regions.

(ii) The following cross-section is one of the possible solutions. Since the test chip already has both NMOS transistors and capacitors, a simple connection between the two is also acceptable as a solution.





Note that the n+ region has to be larger than the contact opening and capacitor area and the gate length has to be larger than the channel to allow patterning alignment errors. The tradeoff of not having self-aligned S/D is excess gate-to-S/D capacitance for the MOSFET.
Since we have no channel stop implant, device isolation is doen by using a relatively thick field oxide.

Process Flow:
1) Spin on phosphorus doped SOG.: n+ region patterning (Mask 1). Drive-in.
2) Strip SOG . Thermal oxidation to form field oxide.
3) Gate oxide patterning after field oxide growth (Mask 2). Grow thin gate oxide.
4) Contact opening (Mask 3)
5) Alunminum deposition.: Metal patterning (Mask 4)

Problem2 General Questions

(a) (i) Increasing substrate concentration will decrease both x_{dmax} and junction depth x_j. Both reductions will reduce lateral depletion charges underneath the gate contributed by the S/D junctions. Therefore less short channel effect.

Reducing gate oxide thickness has no effect according to the Yau model especially when VD is small.

[Optional answer (more advanced) : The vertical electric field created by the gate is larger when oxide is thinner. The lateral electric field contributed by the S/D junctions is relatively less. Therefore less short channel effect , especially for larger VD bias.

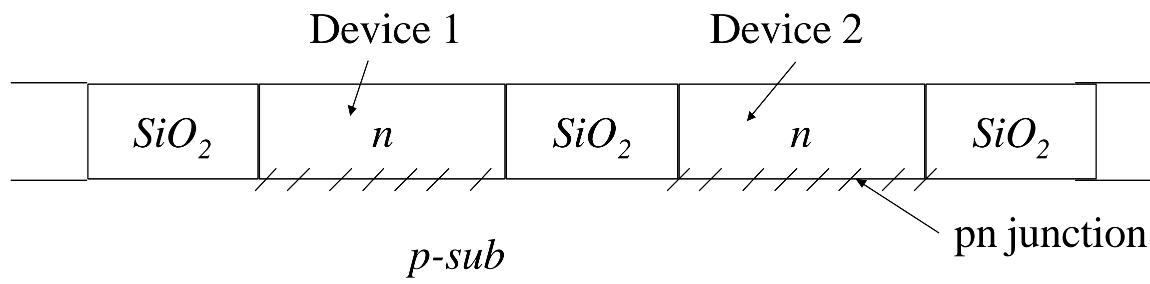
(b) Local removal rate is proportional to the local normal pressure exerted by the pad and slurry on the substrate according to the Preston Equation. Corners of local protrusion has a higher normal pressure than flat surface and will be removed faster than the flat area. With continuous removal, the protrusion area will eventually be planarized with the flat area.

(c)

(i) The pockets of SOG are used for partial planarization.

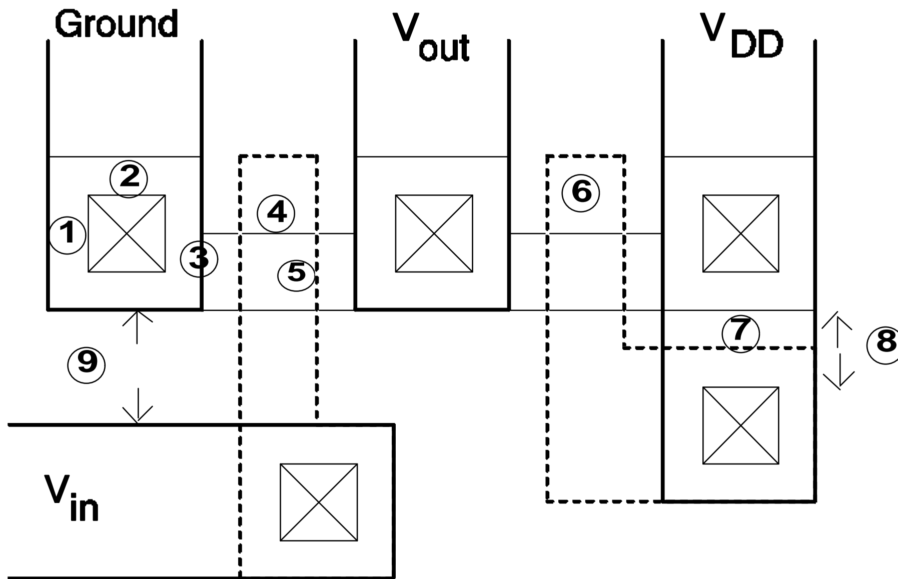
(ii) Because Al is already present when nitride is deposited, the nitride is put down by PECVD which does not have perfect conformal coverage when deposition temperature is relatively low.They form the "keyholes" especially when the gap has higher aspect ratios. Substrate bias during PECVD can create resputtering from the deposited films and give better step coverage. The chemical recipes can also be changed to enhance more surface diffusion.

(iii) Oxide trench isolation



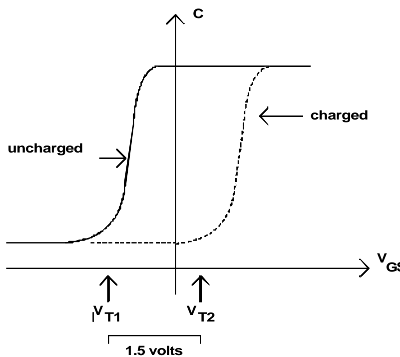
(iv) Since Al-alloy is not easy to be deposited with CVD for precise Cu content, it is deposited by sputtering. To avoid Al melting, the MoSi2 has be deposited at low temp also. Sputtering is also preferred. To have better planarization, W plugs can be used.

Problem 3



1. **Min contact hole =** 2λ
2. **Min contact overlap =** λ
3. **Min contact to gate =** 2λ
4. **Min gate length =** 2λ
5. **Min gate width =** 2λ
6. **Min gate overlap of field oxide =** 2λ
7. **Min poly to diffusion =** λ
8. **Min poly contact to thin oxide =** 2λ
9. **Min metal to metal =** 3λ

Problem 4



a.) $\Delta V_T = 1.5 \text{ volts} = \dfrac{-Q_{electrons}}{C_{ox}}$

$\therefore Q_{electrons} = -1.04\times10^{-7}$ Coulombs/cm^2

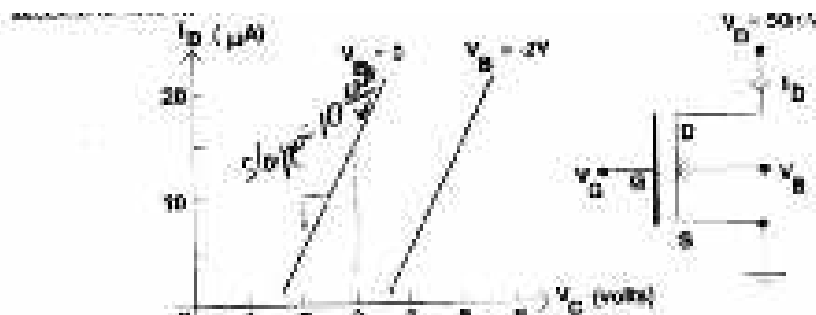
b) Let $V_{T1} = V_T$ for uncharged state

$$|\phi_p| = +0.288 \text{ volts} ;\ V_{FB} = -0.888 \text{ volts} ;\ V_{ox} = \frac{\sqrt{4\varepsilon_s q N_a |\phi_p|}}{C_{ox}} = 0.20 \text{ volts} ;\ V_{Si} = 2|\phi_p| = 0.576 \text{ volts}$$

$$\therefore V_{T1} = V_{FB} + V_{ox} + V_{Si} = -0.112 \text{ volts}$$

$$\therefore \text{ Sensing gate voltage} = \frac{V_{T1} + V_{T2}}{2} = 0.64 \text{ volts}$$

Problem 5



(a)(5 points) Find the threshold voltages for (i) $V_B=0$ and (ii) $V_B=-2V$

$V_T(V_B=0) = 1.5V$, $V_T(V_B=-2V) = 3.5V$

(b)(5 points) Find the substrate doping concentration (assume the substrate is uniformly doped).

$\gamma = \frac{\sqrt{2\varepsilon_s q N_A}}{C_{ox}}$, $\Delta V_T = \gamma\left[(2|\phi_p| + V_{SB})^{1/2} - (2|\phi_p|)^{1/2}\right]$

Using my calculator: $N_A \approx 2.3\times10^{?}\ cm^{-3}$

Check: $\gamma = 2.53$, $\phi_p = 0.371 \Rightarrow \Delta V_T = 2.53\,[(0.741+2)^{1/2} - (0.741)^{1/2}]$

(c)(5 points) Find the carrier mobility in the channel

$I_D \approx \mu_n C_{ox}\left(\frac{W}{L}\right) V_{DS} V_{GS} \Rightarrow C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.45\times10^{-8}\ \frac{F}{cm^2}$

$\Rightarrow \mu_n = \frac{10\mu A}{V} \cdot \frac{1}{C_{ox}\left(\frac{W}{L}\right) V_{DS}} = 580\ \frac{cm^2}{Vs}$

(d)(5 points) Find I_{Dsat} of the transistor for $V_B=0$ and $V_G=10V$

$V_T(V_B=0) = 1.5V$

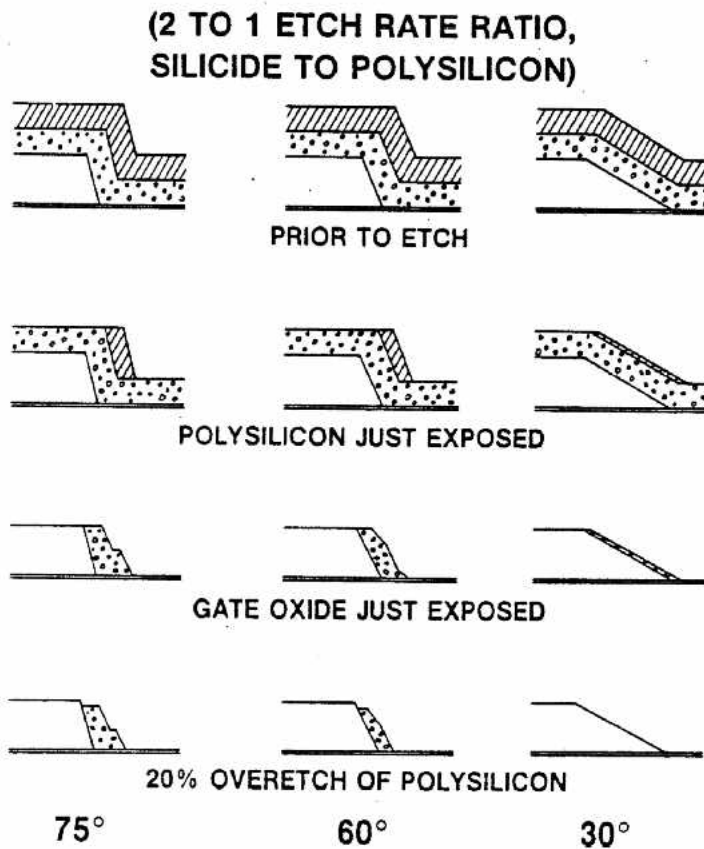
$\Rightarrow I_{Dsat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_G - V_T)^2$

$= \frac{1}{2}(580)(3.45\times10^{-8})(10)(8.5)^2$

$= 7.23\ mA$

Problem 6

(a)



(b)

(i) O atom (and possibly O_2 molecules) destroy the concentration of unsaturated CF_x, increases the F/C ratio. Therefore etching increases. In addition, reactions like:
$O + CF_3 \rightarrow COF_2 + F$ and $O + CF_2 \rightarrow CO + 2F$ etc.. will give free F radicals which also increases the etching rate.

(ii) This is believed to be due to oxygen dilution effects; i.e. the flow of F atoms into the discharge is reduced by the % of oxygen in the feedstock.

Problem 7 MEMS

the scan length.

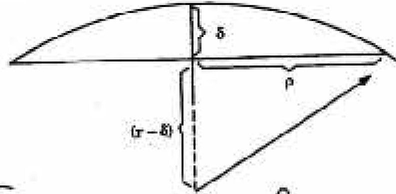
(b) Given a scan length of 5 cm and a bow of 20,000 Å calculate the stress for an unknown film 2 μm thick. The substrate is a 200 μm thick Si wafer ($Y/(1-\nu)$ for (100) Si $= 1.8 \times 10^{11}$ N/m²).

from figure: $r^2 = (r-\delta)^2 + \rho^2$

then $r = \dfrac{\rho^2 + \delta^2}{2\delta}$

Since $\rho \gg \delta$ $\quad r = \rho^2/2\delta$

then $\dfrac{1}{6r} = \dfrac{1}{6} \times \dfrac{2\delta}{\rho^2} = \dfrac{\delta}{3\rho^2}$ as required.



b) scan of 5 cm and bow $2\times10^{4}\times10^{-10}\,m = 2\times10^{-6}\,m$

$\rho = (2.5\times10^{-2}\,m)$

$$\sigma = \left(\frac{2\times10^{-6}\,m}{3\,(2.5\times10^{-2})^2}\right)\times\left(1.8\times10^{11}\,N/m^2\right)\times\frac{(200\times10^{-6}\,m)^2}{2\times10^{-6}\,m}$$

$= 3.84\times10^{6}\,N/m^2$

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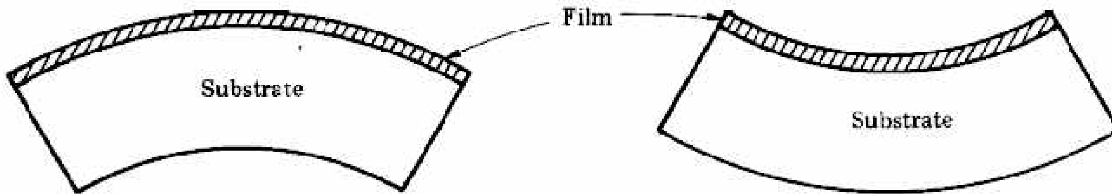

(a) Compressive stress (b) Tensile stress

(b) Process flow – any consistent process flow will do.