Fall 2003

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE143 Midterm Exam #2

Family Name _____ First name_____

Signature_____

Make sure the exam paper has 7 pages including cover page

This is a 90-minute exam (8 sheets of notes allowed)

DO ALL WORK ON EXAM PAGES

Whenever possible, use sketches to illustrate your explanations.
Numerical answers orders of magnitude off will receive no partial credit.

Problem 1 (25 points)_____

Problem 2 (25 points)_____

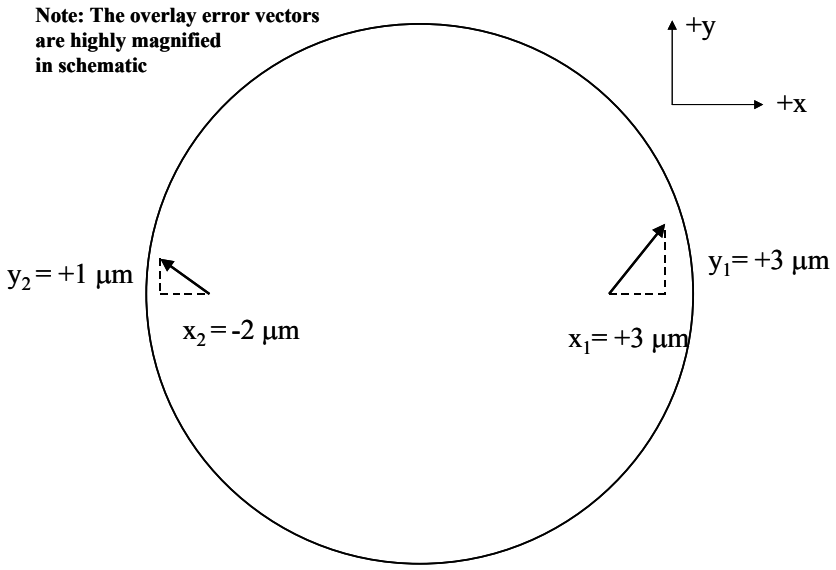
Problem 3 (20 points) _____

Problem 4 (30 points) _____

TOTAL (100 points) _____

Problem 1 Lithography (25 points total)

(a) We only measure the overlay errors for the Right and Left alignment marks near the edge of a 100mm-diameter wafer.



	Top	Right	Center	Left	Bottom
x	Not measured	+3 μm	x_t (Not measured)	-2 μm	Not measured
y	Not measured	+3 μm	y_t (Not measured)	+1 μm	Not measured

(i) (3 points) Calculate the x and y components of the translational error (x_t , y_t)

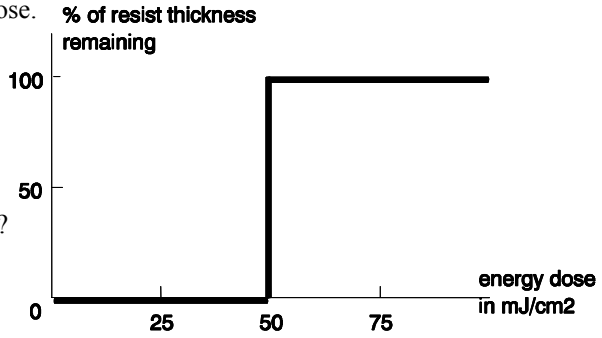
(ii) (2 points) Calculate the thermal run in / run out error

(ii) (2 points) Calculate the rotational error- also indicate clockwise or counterclockwise in answer.

Problem 1 Lithography continued

(b) (4 points) For projection lithography, the printable resolution $R = k \times \frac{\lambda}{NA}$ and depth of focus $DOF = \frac{\lambda}{2NA^2}$. The k-factor is known as the technology factor since it depends on both diffraction and resist effects. Suppose we improve on the resist technology such that k is reduced by 20%. For fixed λ and fixed R, calculate the percentage change in DOF.

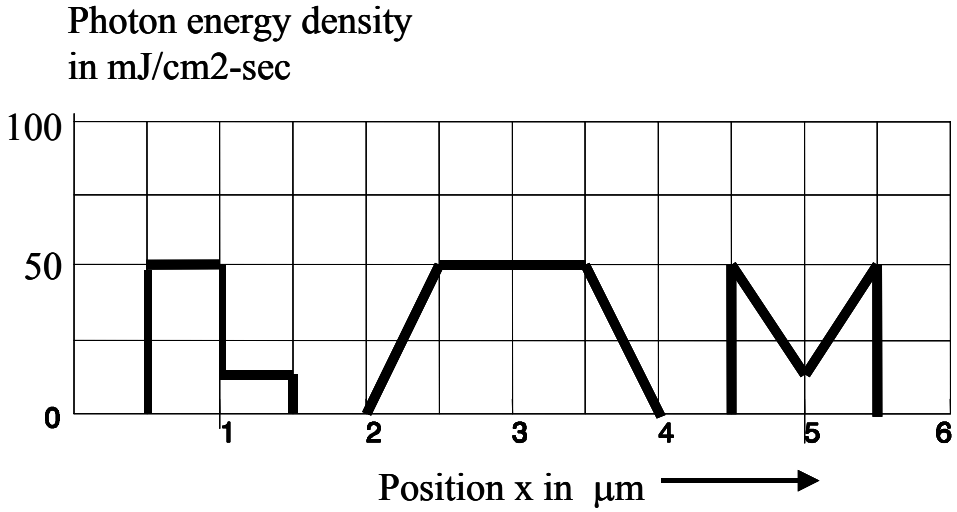
(c) A photoresist has the following response to photon energy dose.



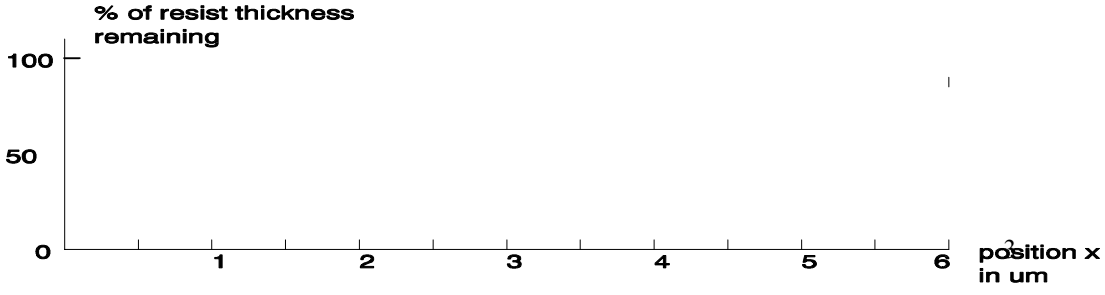
(i) (2 points) Is this a positive or negative resist.

(ii) (2 points) What is the value of the resist sensitivity ?

(iii) (10 points) The resist described in part(c) is exposed to the following aerial image intensity profile I(x) [in mJ/cm^2 –sec]



Sketch below the cross-section of the resist after development with an exposure time of 2 seconds.

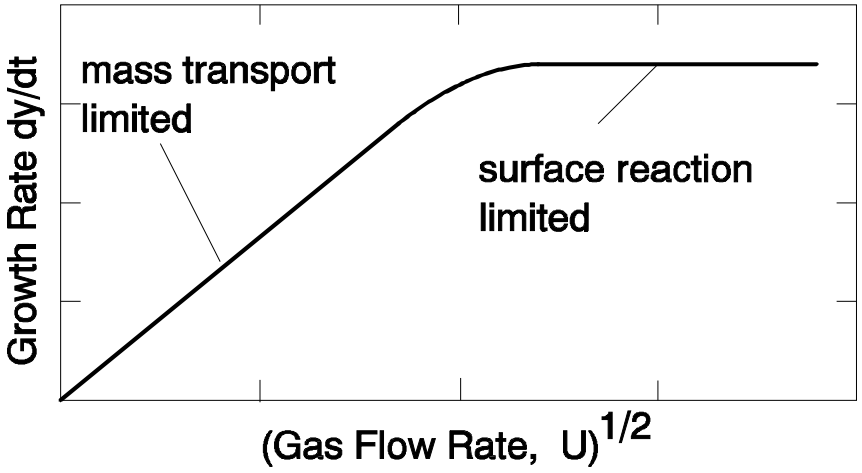


Problem 2 Thin Film Deposition (25 points total)

(a) (4 points) For thin-film deposition on nonplanar surfaces using directional flux, one will experience geometrical shadowing effect and self-shadowing effect. Explain the difference.

(b) (4 points) A CVD process deposition rate is known to be surface-reaction limited between 600 ^{o}C to 900 ^{o}C. The deposition rate at 700 °C was found to be 2000 Å /min and the deposition rate at 800 °C was found to be 20000 Å /min. Calculate the activation energy of the surface reaction mechanism. [Given : Boltzmann's constant $k = 8.617 \times 10^{-5}$ eV/K]

(c) The following sketch shows a plot of the CVD growth rate versus the square root of the gas flow velocity at a given temperature.



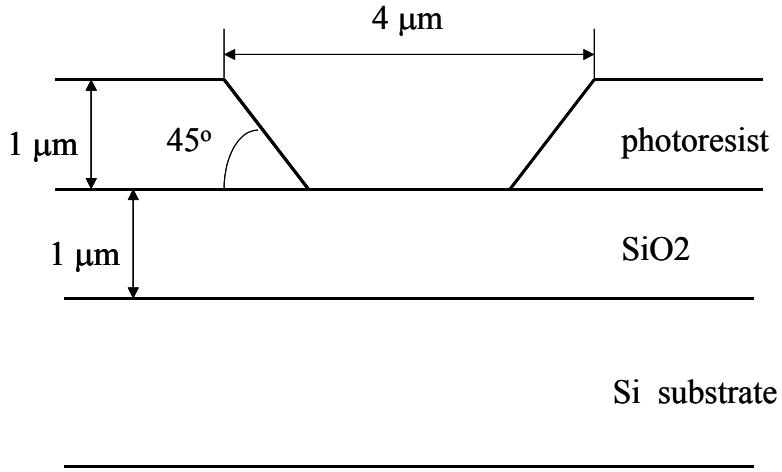
Suppose all other CVD control parameters are the same **except the temperature is higher**.
(i) (3 points) Discuss how the surface reaction limited regime is affected by raising the temperature.

(ii) (4 points) Discuss how the mass transport limited regime is affected by raising the temperature.

(iii) (6 points) Re-sketch the growth rate curve in the above figure.

(d) (4 points) List several motivations to use plasma enhanced chemical vapor deposition (PECVD) ?

Problem 3 Etching (20 points total)
An reactive ion etching (RIE) process is used to open oxide contact holes. Photoresist is used as the etching mask. The geometry is shown below:



The RIE process has the following etching characteristics :

	Vertical etching rate	**Degree of Anisotropy**
Photoresist	0.2 μm /min	0
SiO2	1 μm /min	1
Si	0.5 μm /min	1

(a)
(i) (5 points) **In the above figure, sketch the cross-section of all layers after etching for 1 minute.**

(ii) (2 points)Calculate the width of the opening at the top of the contact hole.

(iii) (2 points) Calculate the width of the opening at the bottom of the contact hole.

(b) Suppose the SiO_2 thickness has a variation of ±20% and SiO_2 etching rate has a variation of ±10%.
(i) (3 points) Use worst-case design consideration to find the **minimum** etching time to clear all contact holes on a wafer.

(ii) (3 points) Use worst-case design consideration to calculate the **maximum** depth of Si substrate being etched.

(b) (5 points) The above RIE process uses a pure CF_4 plasma. By adding hydrogen to the CF_4 plasma , one can reduce the Si substrate being etched during the over-etch time. Briefly describe the mechanisms involved.

Problem 4 Metallization and Planarization (30 points total)

(a) (6 points) To etch Aluminum lines using reactive ion etching, one have to use a sequence of three processing steps. Name these steps and briefly describe the recipe and purpose of these steps.

Step1 –

Step 2 –

Step 3 -

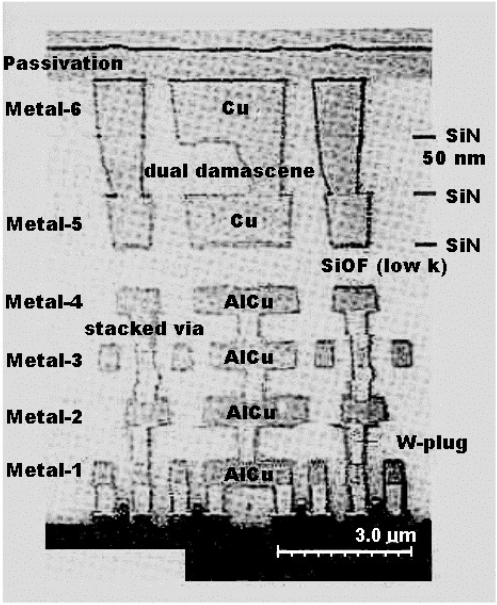
(b) (6 points) Spin-on-glass (SOG) is often used as a dielectric to planarize metallization systems. Sketch a simple process flow to illustrate how it is being used.

List a couple advantages of using SOG----

List a couple of disadvantages of using SOG ----

Problem 4 continued

(c) The photograph below (taken from the textbook Jaeger) shows the cross-section of a multilevel metallization system using four layers of aluminum-copper interconnections with tungsten plugs plus two levels of dual Damascene copper interconnection.



(i) (10 points) Name the deposition methods and patterning methods for the following material structures:

	Deposition Method	**Patterning Method**
AlCu interconnect		
W-plug		
SiN etch stop		
Cu interconnect		
Cu plug		

(i)(2 points) What is the typical Cu content (in atomic percent) of the Al-Cu alloy ? Why do we use the Al-Cu alloy as an interconnect material ?

(ii) (2 points) What is the purpose of using the W-plugs ?

(iii)(2 points) What is the purpose of using the SiOF dielectric to isolate metal layers?

(iv) (2 points) Why do we need the SiN etch stop layers for the Dual Damascene process? Illustrate with sketches if possible.