# EE143 Fall 2004 Midterm 1 solutions

**Problem 1**

(i ) Three lithography steps are used in this process flow.

Mask 1: Pattern Poly-1 hinge plate
Mask 2: Pattern the staple anchor openings through bottom PSG
Mask 3: Pattern the Poly-2 staple

(ii) Four CVD steps are used:

CVD1- bottom PSG deposition
CVD2- poly-1 deposition
CVD3- top PSG deposition
CVD4- poly-2 deposition

(iii ) Four thin-film etching steps are used:

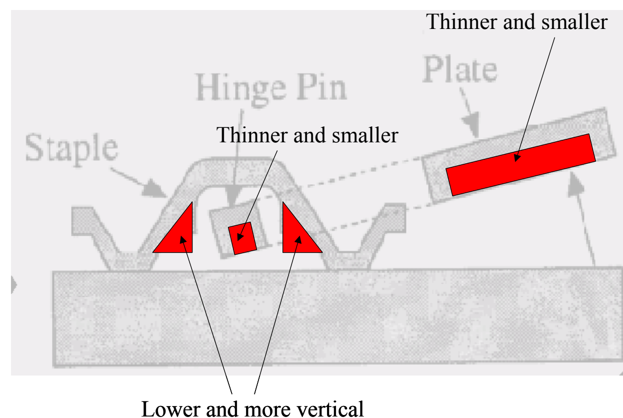
Etch 1: Etch Poly-1( hinge plate)
Etch 2: Etch staple anchor openings through bottom PSG
Etch 3: Etch Poly-2 (staple)
Etch 4: Etch all PSG sacrificial layers to release hinge

(iv) NO. Part of the hinge structure is **underneath** the staple structure. If staple is formed first, there is no way to pattern the hinge outline (litho and etch) AND no way to deposit the part of poly-1 which is underneath the staple structure.

(v) AGREE. There is no high-temperature processing steps used after Al deposition, Al melting is a non-issue.
[Optional answer: DISAGREE. One has to find a proper wet/plasma etching recipe with the right selectivity to etch PSG without attacking Al.]

(vi) Major differences (schematic shown below: red is structure using poly-1 oxidation) :

(1) poly-1 plate thinner ( poly-Si is consumed during thermal oxidation)
(2) cross-section of poly-1 under staple area is smaller (affects poly-1 & poly-2 gap spacing under staple)
(3) staple cross-section has more vertical sidewalls because there is no PSG (layer 1).



**Problem 2**

(a) (i) $A = B/(B/A) = 0.027 / 0.178 = 0.152\ \mu m$

$$x_{ox}^2 + Ax_{ox} = B(t + 0)$$

For $x_{ox} = 0.2\ \mu m$, $0.2^2 + 0.152 \times 0.2 = 0.027 \times t$

$\Rightarrow$ **t = 2.6 hrs**

(ii) From 1000 °C, wet oxidation curves :
With no initial oxide, it takes ~ 0.3 hrs to form 0.2 µm of oxide.
With no initial oxide, it takes ~ 1.4 hrs to form 0.5 µm of oxide.
Starting with 0.2 µm of oxide, it takes (1.4-0.3) =**1.1 hrs** to form an additional 0.3 µm of oxide.

(b) If final thin oxide thickness is < 100nm, one empirical way to correct the Deal-Grove model prediction is to used an initial oxide thickness $x_i$ ~20nm instead of zero even when the starting wafer has no initial oxide.

For very thin oxides (tens of nm) , one can also modified the Deal-Grove growth rate to :

$$\frac{dx_{ox}}{dt} = \frac{B}{A+2x_{ox}} + C \bullet \exp[-x_{ox}/L]$$ where is L ~7 nm.

Note that the empirical exponential term is only significant for small $x_{ox}$. This additional term goes to zero when $x_{ox}$ is large.

(c ) HCl reacts with oxygen to generate water molecules: $4HCl + O2 \rightarrow 2H_20 + 2Cl_2$ . The created $H_20$ adds a faster oxidation mechanism (i.e. steam oxidation) to the dry-oxygen oxidation mechanism. Cl also increases the interface reaction with an increase of $k_s$.

**Problem 3**

(a) $(0.6 - \Delta) \bullet 2.17 = 0.6 \Rightarrow$ **$\Delta$ = 0.324 µm**

(b) (i) If $R_p = 0.6\ \mu m$ , half of the implanted dose will be inside Si and half of dose will be inside $SiO_2$. For $B^+$ions, we need ~**220 keV** ion energy.
The corresponding $\Delta R_p$ is ~ 0.1 µm

(ii) $C_p = \dfrac{2 \times 10^{13}}{\sqrt{2\pi}\Delta R_p} = 8 \times 10^{17}/cm^3$

$$(x_j - R_p)^2 = 2\,(0.1)^2 \bullet \ln\left(\frac{8\times10^{17}}{10^{15}}\right)$$

$\therefore$ $\mathbf{x_{j2}} = R_p + 0.365\ \mu m$ **= 0.965 µm**

(iii ) Using $\mu_p$ ~ 160 cm$^2$/V-sec at $Cp = 8\times10^{17}/cm^3$
and $R_S \sim 1/(q\,\mu\,\phi_{Si}) = 1 / (1.6 \times 10^{-19} \times 160 \times 1 \times 10^{13})$ **= 3900 ohm /square**.

(c)

**Underneath Si3N4 region**
The nitride is given to be thin. One can ignore its ion scattering effects. Since the ion beam is aligned along the Si (100) channeling direction, most ions will experience ion channeling effect when traversing the crystalline Si substrate.

**Underneath SiO2 trench:**
SiO2 is amorphous ; ions will be scattered randomly when traversing the thick SiO2 layer. When ions reach the crystalline Si substrate, majority of ion paths are no longer along the (100) channeling direction of crystalline Si. Therefore, less ion channeling.

Conclusion:
**$x_{j2}$ is deeper undernetah the Si3N4 region than $x_{j2}$ underneath the SiO2 region.**

(d) One example which was shown in Jaeger : When forming the source/drain of a MOSFET using implantation, the lateral straggle $\Delta R_t$ will give a larger lateral spread of dopants underneath the poly-Si gate. The resultant channel length L of the MOSFET is shorter.