Spring 2003

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS143 Final Exam

Family Name ________________________ **First name**____________________________

Signature____

Instructions: DO ALL WORK ON EXAM PAGES

Make sure your copy of the exam paper has 12 pages (including cover page)
This is a 3-hr exam (12 sheets of notes allowed)

Grading: Whenever possible, use *sketches* to support your explanation.
Show correct units and algebraic sign for numerical answers.
No partial credit for numerical answers orders of magnitude off.

Problem 1 (40 points)________________

Problem 2 (20 points)________________

Problem 3 (30 points) ________________

Problem 4 (30 points) ________________

Problem 5 (25 points) ________________

Problem 6 (30 points) ________________

Problem 7 (25 points) ________________

TOTAL (200 points) __________________

Information which may be useful

$\varepsilon_s = 1.036 \times 10^{-12}$ F/cm for Si

$\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm for SiO_2

$q = 1.6 \times 10^{-19}$ coulombs

Boltzmann constant $k = 8.62 \times 10^{-5}$ eV/K

n_i of Si= 1.45×10^{10} cm^{-3} at 300K

E_g of Si = 1.12 eV at 300K

Electron Affinity of Si =4.15 eV

Electric potential $\phi = (E_f - E_i)/q$

$n = n_i \exp(q\phi/kT)$

$$x_d = \left[\frac{2\varepsilon_s}{q} (\phi_i - V_a) \left(\frac{1}{N_a} + \frac{1}{N_d}\right) \right]^{1/2}$$

MOS: $V_{GB} = \phi_{MS} + V_{ox} + V_{Si}$

$$V_{FB} = \phi_{MS} - \frac{1}{C_{ox}} \left[Q_f + \int_0^{x_{ox}} \frac{x \, \rho_{ox}(x)}{x_{ox}} dx \right]$$

MOSFET I-V (n-channel):

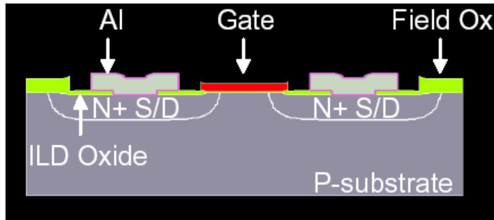
$$I_{DS} = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_T) V_{DS} - V_{DS}^2/2 \right]$$
(below saturation)

$$I_{Dsat} = \mu_n \frac{W}{L} C_{ox} \left[(V_G - V_T)^2/2 \right]$$ (above saturation)

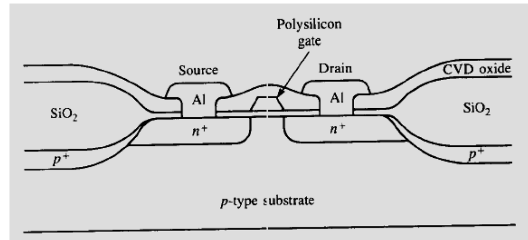
Problem 1 Lab Questions (40 points total)

(a) (6 points) The following cross-sections show the NMOS transistors you made in the EE143 Lab and those made with the generic process as described in the textbook (Jaeger).

EE143 NMOS Transistor



Generic NMOS transistor described in Jaeger



Describe three major process steps which are different in fabricating these two transistors:

(1)

(2)

(3)

(b) (10 points) Make up a minimum set of processing equipment which will be required to fabricate the generic transistor shown in part(a) . Briefly describe their usage. Remark in the 3rd column whether we can we use the existing equipment in Cory 218 to perform the process steps.

Process Equipment needed	**Usage**	**Can we use existing equipment in Cory 218 ? (Yes, No, Non-existing)**

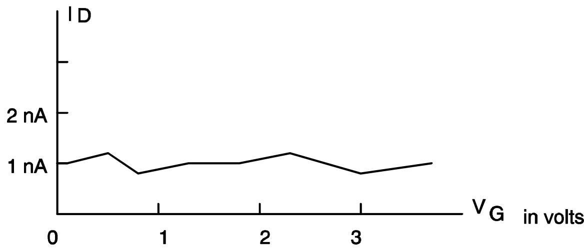
Problem 1 continued

(c) (4 points) In our lab we use Phosphorus as the dopant for the source and drain diffusion. However, most advanced processes use Arsenic. Why do we use Phosphorus is our lab? Why the advanced processes use Arsenic?

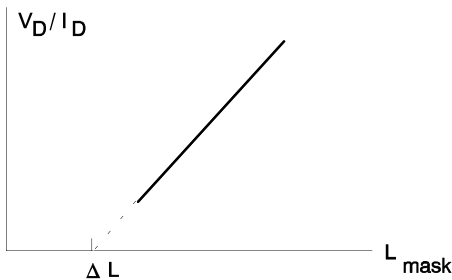
(d) (10 points) In the MOSFETs fabricated in the lab, the actual device dimensions are different from the mask dimensions. State qualitatively (increase [+], decrease [-], or no change [0]) the effect of the following steps on the channel length L and channel width W of the finished devices. Note that we are using positive photoresist in our EE143 process.

	L	W
Increased field oxide thickness		
Longer source/drain drive-in		
Overdeveloped gate photoresist		
Overdeveloped contact hole photoresist		
Overdeveloped metal photoresist		

(e) (4 points) When characterizing the NMOS transistors in the lab with a fixed V_{DS} = 1V, you tried to plot I_D versus V_G and the result looks like the following sketch. What will be your explanation?

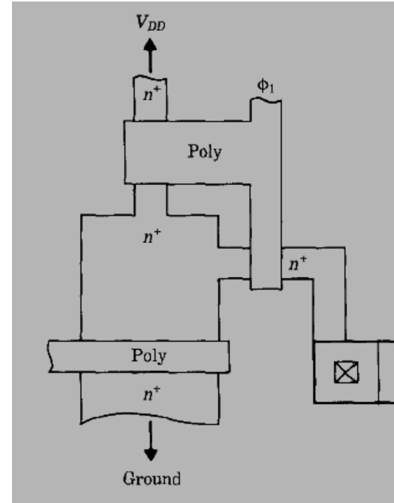


(f) (6 points) On the EE143 chip, we have many transistor sizes indicated by the L_{mask} values. Suppose we ground the source and then apply a small V_D (~0.1V) with a gate voltage higher than V_T (~5V) to measure the drain current I_D for all transistors. The plot of V_D/I_D versus L_{mask} is a straight line. The intercept of this plot with the horizontal axis (L_{mask} axis) gives a value ΔL. What is the physical meaning of ΔL? What processing steps contribute to the value of ΔL?



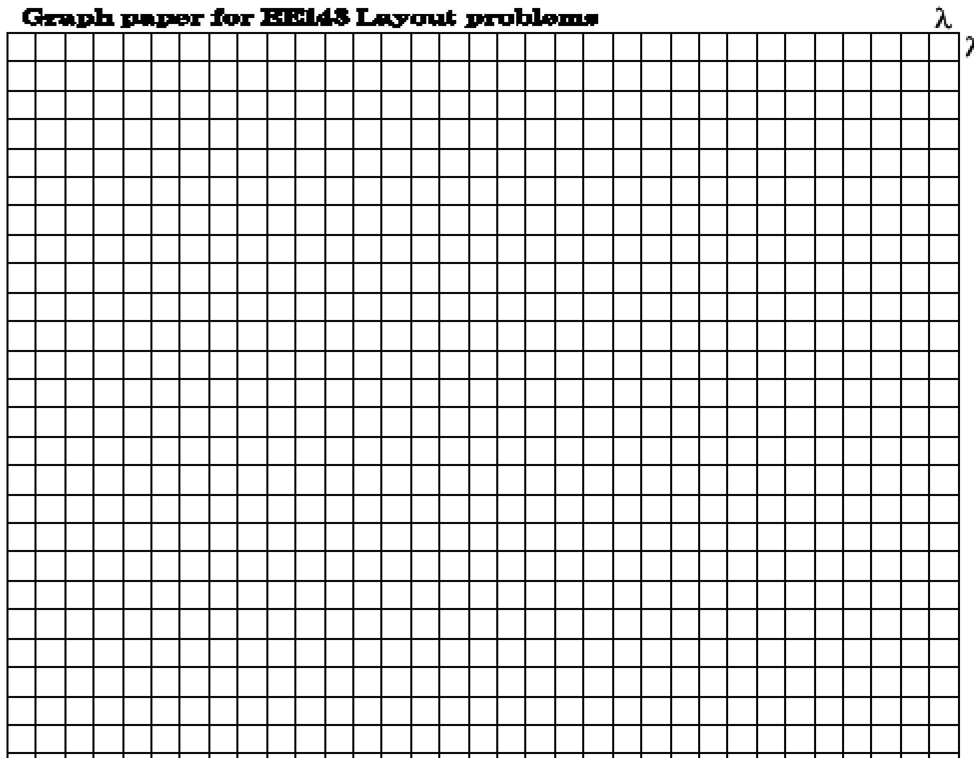
Problem 2 Layout (20 points total)

The following figure shows a schematic top view of an IC layout (not to scale). The metal contacts to V_{DD}, Ground, and ϕ_1 are not shown.



(a) (4 points) how many MOS transistors are there in this circuit?

(b) (16 points) Use our EE143 layout design rules to do a **minimum** geometry layout. Assume all transistors have W=2λ and L =2λ



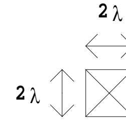
Reference: EE143 Standard Layout symbols and Design Rules

1. Background

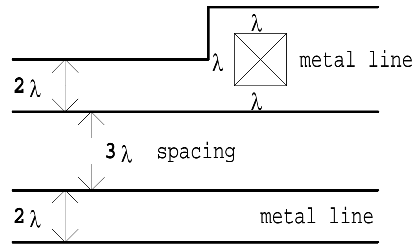
1.1 Lithography/etching limit on minimum feature or spacing = 2λ
1.2 Alignment limit (overlay accuracy) = λ
1.3 Unless specified, default value: λ = 2 μm

2. Symbols and Rules

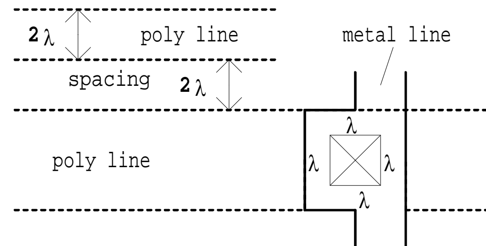
2.1 Contacts (metal to silicon)
minimum size 2λ x 2λ



2.2 Metal
minimum width: 2λ
minimum spacing: 3λ
minimum underlap of contact: λ



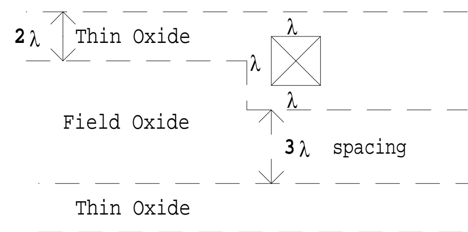
2.3 Polysilicon
minimum width: 2λ
minimum spacing: 2λ
minimum underlap of contact: λ



3. MOS Devices

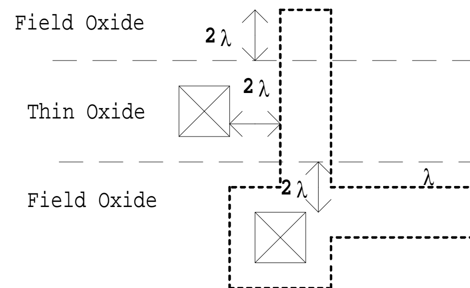
3.1 Thin oxide of MOS
minimum width: 2λ
minimum space: 3λ
minimum underlap of contact: λ

[The thin oxide region is also known as diffusion region. The field oxide region is also called the thick oxide region]



3.2 Si Gate of MOS

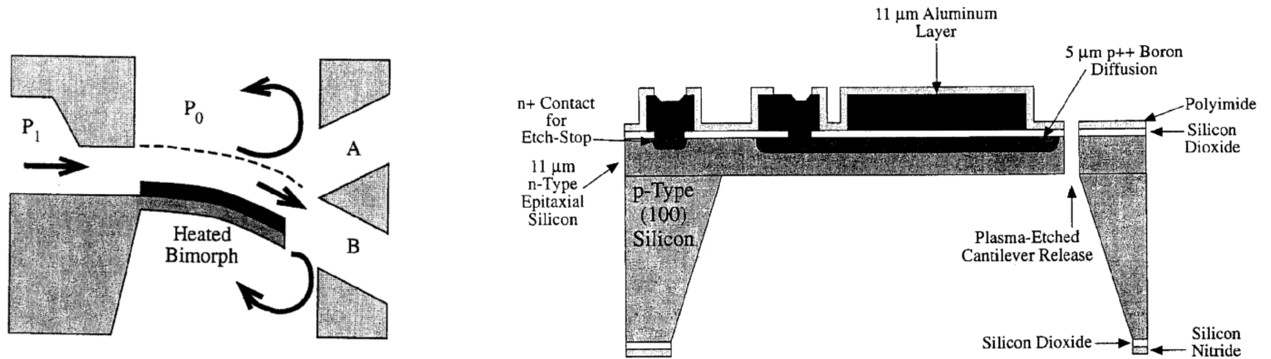
Minimum gate overlap of field =2λ
Minimum contact to gate spacing =2λ
Contacts to polysilicon allowed on thick oxide only. Minimum spacing to thin oxide = 2λ
Minimum poly to thin oxide spacing = λ



Problem 3 MEMS Processing (30 points total)

The following brief description is taken from a MEMS textbook :

"Doering, et al. (1992) demonstrated a thermal bimorph cantilever that combined the use of the Coanda effect with forced convection, to allow a laminar flow to be steered into one of two outlet ports under electrical control (see figure at left). They used an electro-chemical etch-stop and plasma etch edge release to form 11 μm thick n-epitaxial cantilevers that included a p++ boron diffusion for heating resistors and an 11 μm aluminum layer to form the bimorph with silicon (see cross section at right figure)."



Principle of a thermal bimorph cantilever directing fluid flow into one of two outlets

[Background information- The n+ contact for etch stop is an n+ island fabricated on the n-type epitaxial Si. By applying a voltage at the n+ contact during KOH etch of the p-type substrate, etching rate will stop at the pn boundary.]

(a) (6 points) To aid your understanding of how this device operates, draw a top-view of the device. Label all important boundaries.

(b) (4 points) When the p++ resistor pattern is heated up by resistive heating, will the cantilever structure curve upward or downward? Briefly explain.

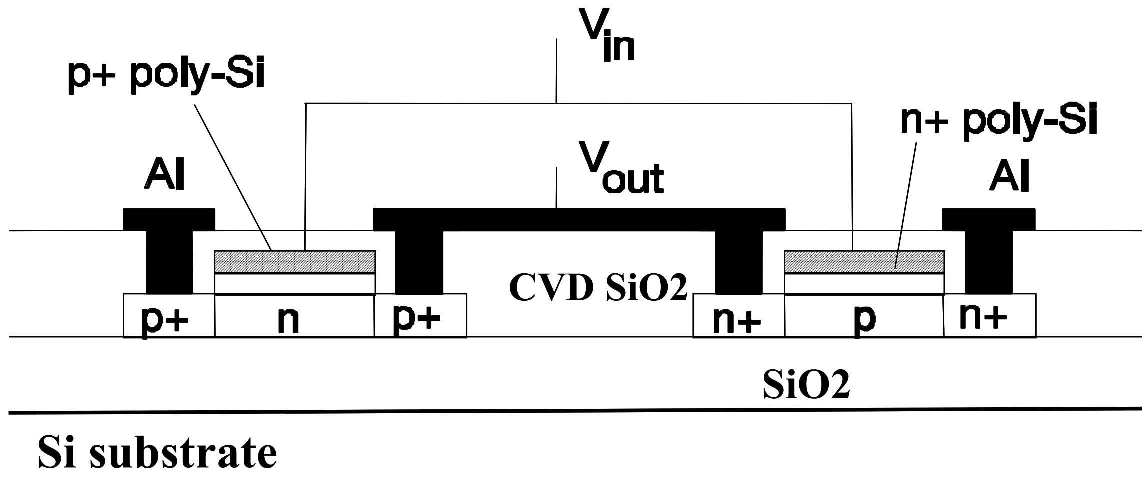
Problem 3 continued

(c) (20 points) Starting with a p-type Si wafer with an n-type epitaxially grown Si, design a process flow to fabricate the bimorph device. Describe the process steps in the left column and sketch the cross-sections in the right column

PROCESS DESCRIPTION CROSS-SECTIONS

Problem 4 MOS Design (30 points total)

(a) The following figure shows the cross-section of a CMOS inverter made with Silicon-on -insulator (SOI) wafers.



(a)(12 points) For the CMOS transistors, the gate oxides are 0.05 μm and oxide and interface charges are assumed to be zero. p^+poly-gate is used for the p-channel device and n^+ poly-gate is used for the n-channel device. If we would like to have V_T (n-channel) = +1volt and V_T (p-channel) =-1V, calculate the required channel doping concentrations for both devices.

(b) (6 points) Keeping the same channel doping concentration for the PMOS but replacing the gate with n+ poly-Si. What will be the new threshold voltage?

(c) (6 points) Suppose we would like to restore the threshold voltage of the PMOS described in part (b) to –1V again by performing a threshold tailoring implantation step in the process flow. What doping specie will you choose? What will be the required dose?

(d) (6 points) The process flow for the CMOS on SOI is much simpler that of CMOS on bulk substrate. List the major process steps which can be skipped.

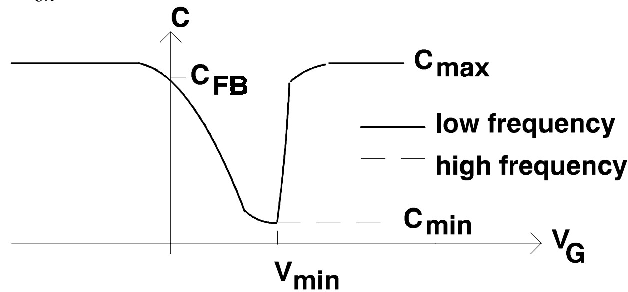
Problem 5 MOS IV and C-V (25 points total)

(A) (a) (6 points) Due to cosmic radiation, the interface charge Q_f at the Si/ SiO_2 interface increases with time for a **NMOS** transistor. The initial threshold voltage is +0.7 volts and decreases linearly with time to 0 volts in 3 years. The n-channel MOS transistors have an oxide thickness of 1000 Å and a substrate doping concentration N_a of 10^{15}/ cm^3. Find the increase of Q_f per year.

(b) (6 points) The fresh MOSFETs of part (a) have I_{Dsat}= 2 mA for V_G=5 volts, V_S= 0 volt, and V_B (body bias) =0 volts. Use Find I_{Dsat} after 2 years.

(c) (6 points) After the threshold voltage has changed to 0 volts after 3 years, you would like to restore the threshold voltage to +0.7 volts by applying a bias V_B to the p-substrate. Calculate the sign and magnitude of the required substrate bias. [The sources of the transistors are grounded.]

(B) (7 points) The p-substrate of an n-channel MOS capacitor has a doping concentration of N_a =5 $\times 10^{15}$/ cm^3. The oxide thickness x_{ox} is 600 Å. The C-V curve is plotted below:



Find the ratio C_{min} / C_{max} .

Problem 6 General Process Integration Questions (30 points total)

(a) (6 points) Describe how to fabricate a **retrograde well** for CMOS. What are the advantages of using the retrograde well?

(b) (6 points) Formation of an oxide spacer is a critical step in the formation of LDD and SALICIDE structures. What are the important process considerations to control the cross-sectional dimensions of the oxide spacer?

(c) (6 points) Show the approaches to etch a vertical sidewall trench into a Si wafer with high aspect ratio.

Problem 6 continued

(d) (6 points)
Compare the two process flows: a tungsten plug process and a single-damascene copper process for contact via fill.

(e) (6 points) For surface topography (e.g. trenches) with different aspect ratios, one will encounter planarization problems using conformal CVD followed by (i) etch back or (ii) CMP. Illustrate with sketches on what the problems you will expect.

Problem 7 State-of-the-art Processing (25 points total)

Discuss qualitatively your understanding of the following process modules:

	Motivations	**Challenges and issues to be resolved**
Extreme UV Optical Lithography		
Ultra Shallow Junctions		
Chemical Mechanical Polishing		
Low-K Dielectrics		
300-mm Si wafers		