NAME (please print) _____

STUDENT (SID) NUMBER _____

UNIVERSITY OF CALIFORNIA, BERKELEY

College of Engineering
Electrical Engineering and Computer Sciences

EECS 145M: Microcomputer Interfacing Lab

LAB REPORTS:

1 _____   2 _____   3 _____

8 _____   9 _____   10 _____

21 _____   22 _____   23 _____

24a _____   24b _____

Total of top 4 Long Lab Grades _____ (400 max)

Total of top 4 Short Lab Grades _____ (100 max)

Lab Participation _____ (100 max)

Mid-Term #1 _____ (100 max)

Mid-Term #2 _____ (100 max)

Final Exam _____ (200 max)

Total Course Grade _____ (1000 max)

COURSE LETTER GRADE

[ ]

Spring 2009 FINAL EXAM (May 15)

Answer the questions on the following pages completely, but as concisely as possible. The exam is to be taken *closed book*. Use the reverse side of the exam sheets if you need more space. Calculators are OK.

Partial credit can only be given if you show your work.

FINAL EXAM GRADE :

1 _____ (15 max)   2 _____ (40 max)   3 _____ (45 max)

4 _____ (45 max)   5 _____ (30 max)   6 _____ (25 max)

TOTAL _____ (200 max)

PROBLEM 1 (15 points)

1.1 (5 points) State the Fourier convolution theorem

1.2 (10 points) Use the Fourier convolution theorem to show that the Integral Fourier Transform of a periodic waveform contains only discrete frequencies.

PROBLEM 2 (total 40 points)

2.1   (15 points) Draw the block diagram for the 12-bit half-flash A/D converter, showing and labeling all principal components and interconnecting lines. (*Note:* this converter has two internal flash A/D converters and one internal R-2R D/A converter, and these can be drawn as single boxes).

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2.1 (continued)

2.2 (15 points) Describe the operation of the 12-bit half-flash A/D converter.

2.3 (10 points) If the absolute accuracy of the 12-bit half-flash A/D converter is 1/8 LSB (i.e. 1/8 step size), what can you say about the required accuracy of the resistors in the two internal A/D converters and in the D/A converter?

Problem 3 (45 points) Design a **computer-controlled** system for testing **eight** 12-bit A/D converters.

You are provided with the following:

- eight A/D converters (to be tested eight at a time)
- eight 16-bit tri-state drivers
- a microcomputer with the following:
  - a 16-bit D/A converter with 1/2 LSB absolute accuracy and 10 µs settling time
  - two 16-bit parallel input ports
  - two 16-bit parallel output ports

You may assume the following:

- The 16-bit parallel output port is in "transparent" mode (no handshaking). New data can be written to the port every 2 µs.
- You have a timer function wait(N), that can delay program execution for N µs.
- The A/D converter requires a "start conversion" low-to-high edge signal and after conversion provides an "output data available" low-to-high edge. The A/D converter sets "output data available" low and resets all internal functions when "start conversion" goes low.
- You must wait until the A/D has signaled that its data are ready before reading its output.

Hint: Think about Laboratory Exercise 9 (A/D converters) and how you would automate the measurement and data analysis procedures.

3.1 (15 points) Draw a block diagram of the major components, including two of the eight A/D converters being tested. Show and label all essential data and control lines.

3.2 (10 points) List the steps your program must do to measure the first transition voltage V(0,1) of the first A/D converter (pseudocode is OK, so long as the logic is clear).

3.3 (10 points) How would you determine the maximum linearity error?

3.4 (10 points) With what accuracy could this system measure the quantities in parts **3.2** and **3.3** in units of 1 LSB of the A/D?

PROBLEM 4 (50 points)

Design a system for sampling two different analog waveforms at 100 kHz using *two* Butterworth low-pass filters and *one* 12-bit A/D converter that is read with a *single* 16-bit digital input port.

- When the waveforms are sampled, they must be sampled simultaneously (within 1 ns).
- Your computer uses a real-time operating system so you do not have to worry about system interrupts, and can read an internal 1 MHz counter using the instruction
  time (in microseconds) = get_tick_count
- The computer can execute instructions at a rate much faster than 1 MHz
- The computer has a 16-bit digital output port that your program can write to using the command "put_single_value (dataout)" which takes 1 microsecond
- The 16-bit digital input port can be read using the command "datain = get_single_value" which takes 1 microsecond
- The 12-bit A/D converter has a "start conversion" (low => high) handshaking line.
- When conversion is complete, the A/D "data available" goes low => high
- The A/D output data are valid until "start conversion" is brought low which makes the A/D converter bring "data available" low
- You will use a Butterworth low-pass filter of order 8 and $f_c = 25$ kHz.

Hint: Consider the S/H amplifier and FET analog switch in your design.

4.1 (15 points) Draw a block diagram of your system, showing and labeling all essential components, connections, and signals.

4.2 (5 points) At what frequency f_1 does the Butterworth filter have gain = 0.99?

4.3 (5 points) At what frequency f_2 does the Butterworth filter have gain = 0.001?

4.4 (5 points) What is the minimum sampling frequency that would prevent electromagnetic interference at f_2 aliasing to f_1?

4.5 (15 points) List the steps (hardware and software) to simultaneously sample (within a few ns) the two analog voltages, sequentially read them into computer memory, and repeat the entire process at the sampling rate of 100 kHz.

PROBLEM 5 (total 30 points)

5.1 (8 points) Compare wireless data interfacing technologies WiFi, Bluetooth and ZigBee in aspects of number of nodes, data throughput rate and battery life.

Standard	Wi-Fi™ 802.11b	Bluetooth™ 802.15.1	ZigBee® 802.15.4
Battery Life (long/medium/short)			
Network Size, # of nodes (big /medium/ small)			
Data rate (high/medium/low)			

5.2 (7 points) Briefly describe situations where each of the three technologies would best be used.

5.3 (15 points)
Use the most suitable technology to design a wireless sensor network that allows a wireless base station to read data from 256 wireless end nodes once per second. Each end node has a sensor circuit. These circuits continuously measure physical quantities such as time, temperature, voltage, etc.

Assume that
• The base station includes a host PC and a wireless central node.
• The sensors produce 16-bit digital outputs.
• The distances between the central node and the end nodes are less than 50 meters
• The end nodes are powered by 50mAh coin batteries, which must last for at least one year.

Sketch your design on the next page, including all devices and their network topology.

5.3 (continued)

PROBLEM 6 (total 25 points)

Parts of the body, such as an arm or a leg, weakened by the effects of the stroke, can regain some functionality by repeatedly stretching them (called physical therapy). You are asked to design a real time controller for a robotic physical therapy device.
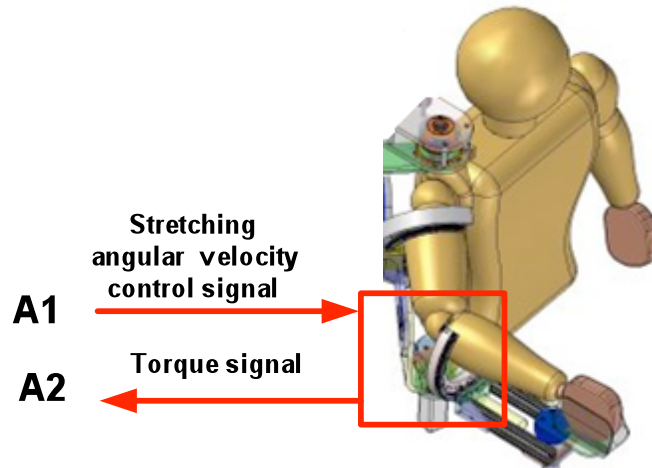
Assume that
- The controller sends analog output signal A1 to control the stretching speed of the robotic device. The stretching speed is proportional to the amplitude of A1. The robotic device rotates in the CCW/CW direction when A1 is plus/minus.
- The controller reads the torque signal back from analog input channel A2. When the absolute value of the torque feedback is larger than a given value, the robotic device must reverse the direction of stretching.

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6.1 (10 points) Draw a block diagram of your interfacing and control system based on the experimental platform you used in your laboratory exercises.

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6.2 (10 points) List the program steps needed to perform the physical therapy motions.

6.3 (5 points) Describe the potential risk to the patient and how you would reduce the risk.