Solutions for Midterm #1 - EECS 145M Spring 1999

1

Name	Interfacing component number
Transparent latch	**3**
Tri-state driver	**4**
Edge-triggered flip-flop	**1**
Sample-and-hold amplifier	**2**

[4 points off for each incorrect entry]

2a
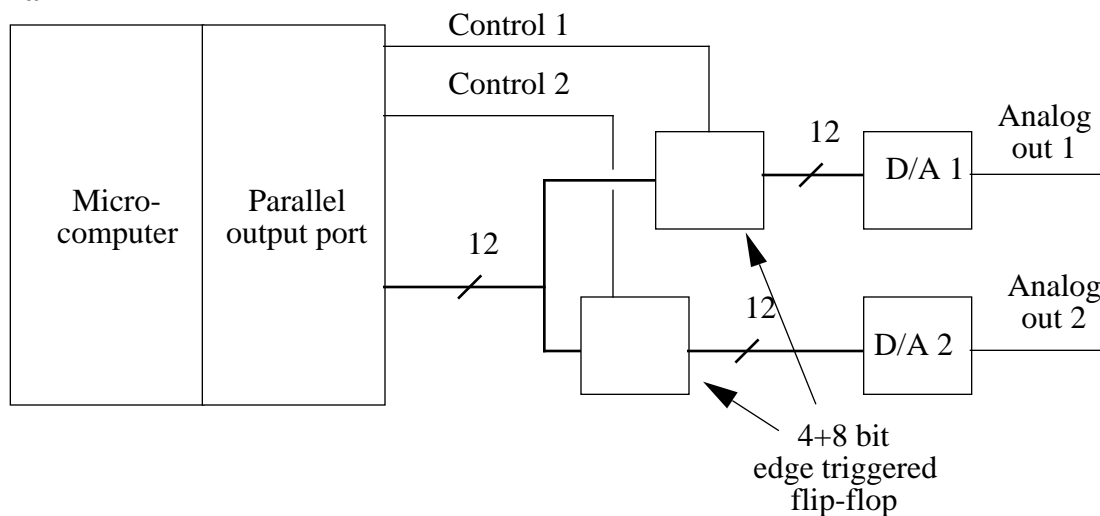
 [4 points off for 8 bits to each D/A (12 were required), leaving none for control]
[4 points off for sending the same number to both D/As]
[2 points off for an 8-bit data bus (12 bits required)]
[2 point off for connecting tri-state buffers to the D/As, since the former have no latching capability]

2b (if using edge-triggered flip-flops)

1   output n1 C1 and C2 low (this asserts n1 on the lines)
2   output n1 with C1 high and C2 low (here n1 appears at the output of flip-flops #1)
3   D/A #1 converts n1 to an analog voltage
4   output n2 with C1 and C2 low (this asserts n2 on the lines)
5   output n2 with C1 low and C2 high
6   D/A #2 converts n2 into an analog voltage
7   output C1 and C2 low

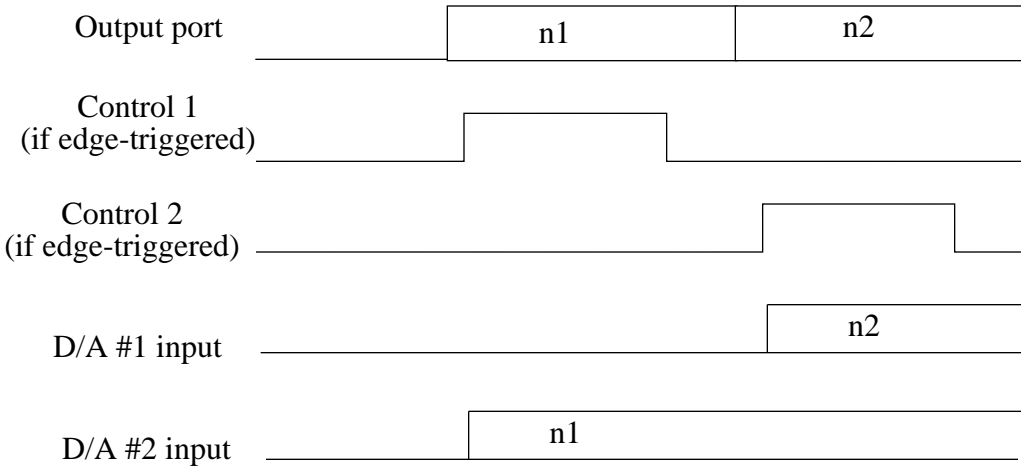**2b** (if using transparent latches)

1   output n1 with C1 high and C2 low (n1 appears at the output of latch #1)
2   D/A #1 converts n1 into an analog voltage

3   output n1 with C1 low and C2 low (latch #1 output is now frozen at n1)
4   output n2 with C1 low and C2 high (n2 appears at the output of latch #2)
5   D/A #2 converts n2 into an analog voltage
6   output n2 with C1 low and C2 low (latch #2 output is now frozen at n2)

[1 point off if the control bits and data bits are not written to the output port in the same operation]
[1 point off if the control bits are written before the data- this will generally latch garbage and the
       D/As will start converting it before the good data arrive]

2c

Output port

Control 1
(if edge-triggered)

Control 2
(if edge-triggered)

D/A #1 input

D/A #2 input

[1 point off if n1 and n2 are not shown as persisting at the D/A inputs until new values are written-
when generating a waveform the D/A inputs must always be desired values]

3a
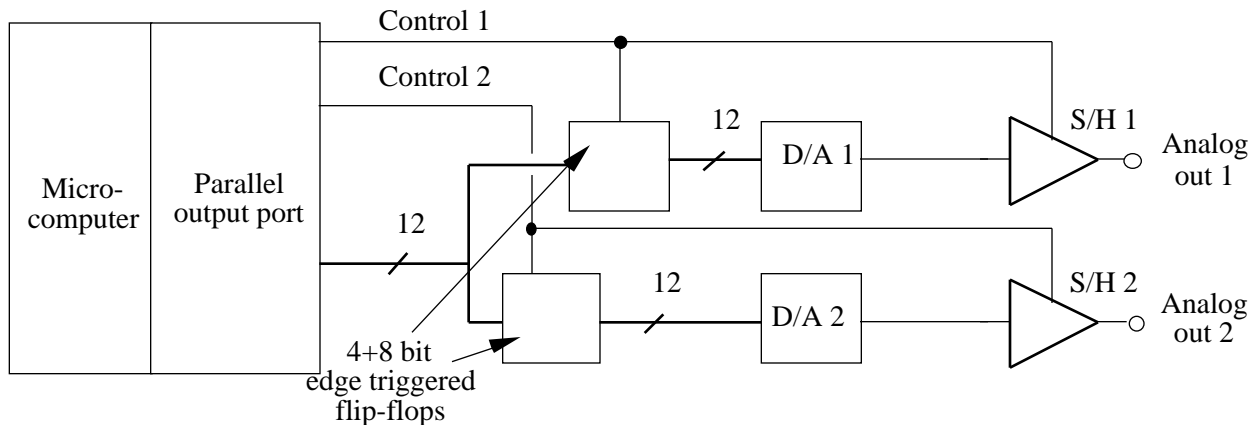
 [6 points off if S/H not at D/A output]
[4 points off if no control lines to S/Hs]
[4 points off if same input always sent to both D/As]
[1 point off for using an additional circuit to sense changes in the D/A input bits and put the S/H
into hold mode during the glitch- this is an unnecessary complexity since this task can be done by
the computer]

3b (if using edge-triggered flip-flops)
1   output n1 with C1 and C2 low (this asserts n1 on the lines)

2   output n1 with C1 high and C2 low (here n1 appears at the output of flip-flops #1 and S/H #1 goes into hold mode)

3   D/A #1 converts n1 to an analog voltage (here is where the glitch occurs)

4   output n2 with C1 and C2 low (this asserts n2 on the lines and puts S/H #1 back into sample mode)

5   analog output #1 (output of S/H #1) changes from the held value to the new stable value of the D/A #1 output

6   output n2 with C1 low and C2 high (here n2 appears at the output of flip-flops #2 and S/H #2 goes into hold mode)

7   D/A #2 converts n2 into an analog voltage (here is where the glitch occurs)

8   output C1 and C2 low (this puts S/H #2 back into sample mode)

9   analog output #2 (output of S/H #2) changes from the held value to the new stable value of the D/A #2 output

3b (if using transparent latches)

1   output n1 with C1 high and C2 low (n1 appears at the output of latch #1 and S/H #1 goes into hold mode)

2   D/A #1 converts n1 into an analog voltage (here is where the glitch occurs)

3   output n1 with C1 low and C2 low (latch #1 output is now frozen at n1 and S/H #1 goes into sample mode)

4   output n2 with C1 low and C2 high (n2 appears at the output of latch #2 and S/H #2 goes into hold mode)

5   D/A #2 converts n2 into an analog voltage (here is where the glitch occurs)

6   output n2 with C1 low and C2 low (latch #2 output is now frozen at n2 and S/H #2 goes into sample mode)
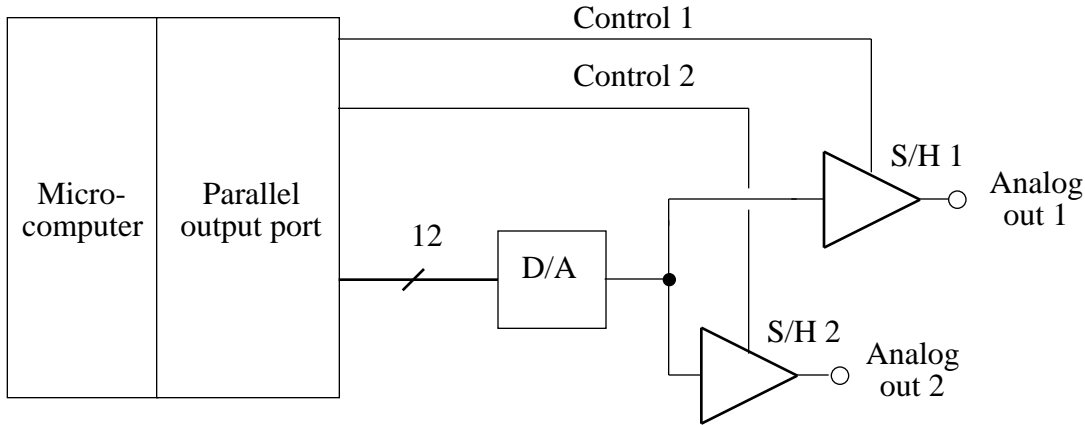
[3 points off if S/Hs not put into hold mode when the corresponding D/A input changes]

3c
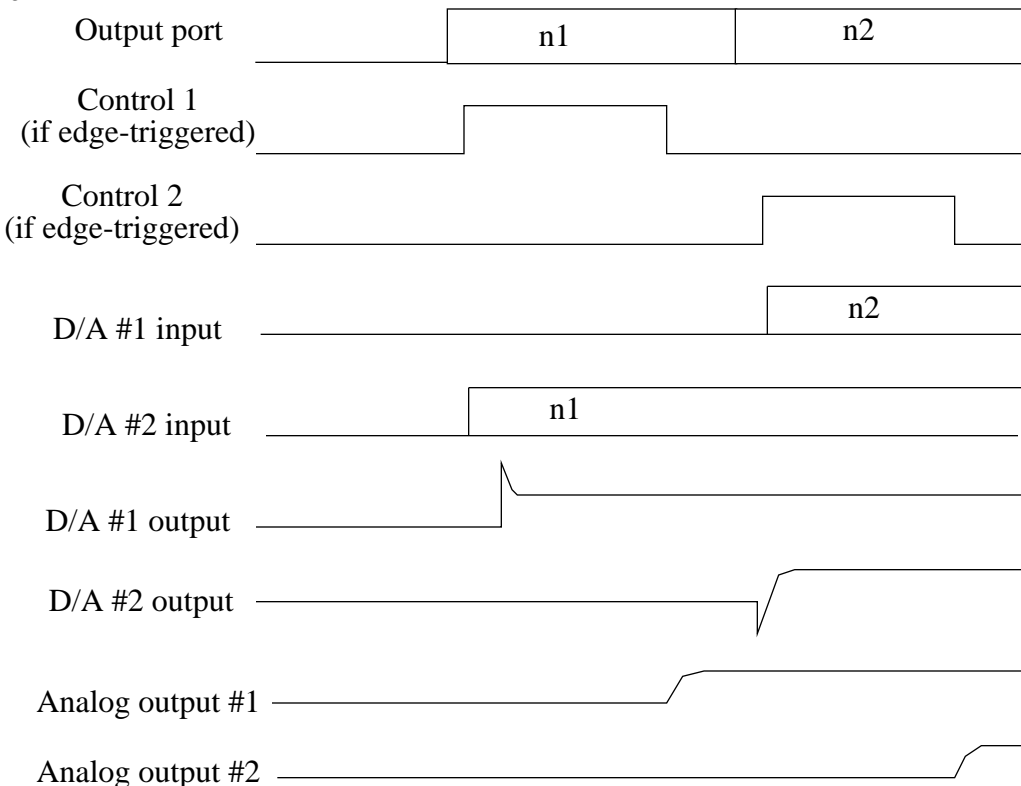
[2 points off if D/A analog outputs (with glitches) not shown]
[2 points off if S/H control not shown]
[2 points off if S/H analog outputs (with glitches gone) not shown]

4a

Control 1

Control 2

S/H 1

Analog out 1

Micro-computer

Parallel output port

12

D/A

S/H 2

Analog out 2

[5 points off if only one analog output line]
[3 points off if S/H control lines not shown]
[1 point off for unnecessary latches between output port and D/A]

4b

1   write n1 with C1 and C2 high (asserts n1 at D/A input and keeps S/Hs in hold mode)
2   after settling, write n1 with C1 low and C2 high (makes analog out 1 equal to stable D/A amplitude)
3   write n1 with C1 and C2 high (freeze n1 amplitude at output of S/H #1)
4   write n2 with C1 and C2 high (asserts n2 at D/A input and keeps S/Hs in hold mode)
5   after settling, write n2 with C1 high and C2 low (makes analog out 2 equal to stable D/A amplitude)
6   write n2 with C1 and C2 high (freeze n2 amplitude at output of S/H #1)

4c

Output port

n1

n2

D/A output

Control 1

Control 2

Analog output #1

Analog output #2
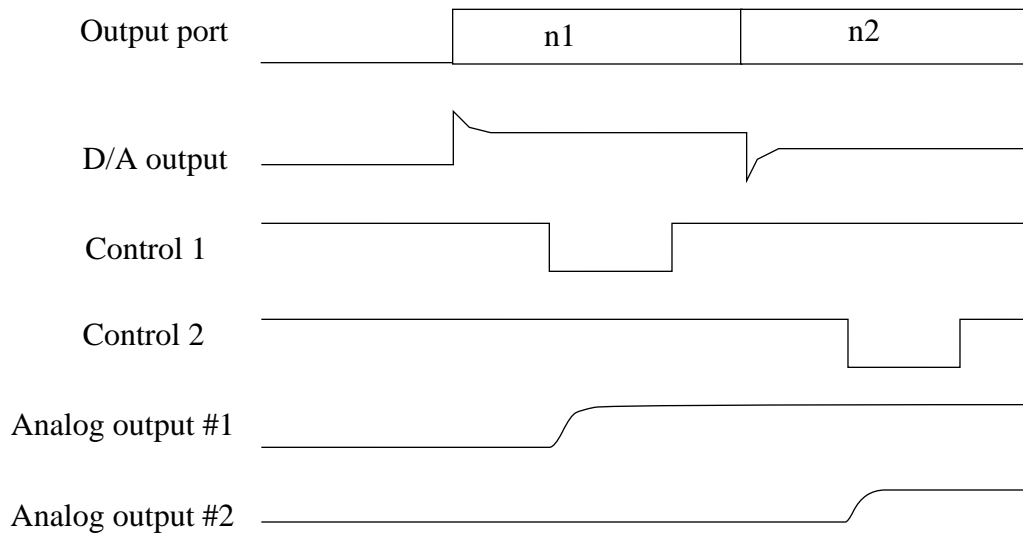
4d
For slow signals whose D/A input values change infrequently, the S/H outputs (which are normally in hold mode) may droop too much before new D/A input values are written. If this is the case, it is necessary to periodically refresh ther S/H output amplitudes by performing the steps in 4b even though the D/A input values are the same.

[3 points off for an irrelevant answer]
[2 points off for creative guessing]
[1 point off for recognizing the S/H droop problem without providing a solution]

Midterm #1 class statistics:

Problem	max	average	rms
1	16	13.9	4.0
2	27	23.2	3.8
3	27	19.3	5.1
4	30	19.0	7.3
total	100	75.4	14.2

Grade distribution:

Range	number	*approximate* letter grade
31-40	1	F
41-50	0	F
51-60	2	D
61-70	6	C
71-80	6	B
81-90	6	A
91-100	4	A