UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

E. Alon	**Midterm**	**EECS 240**
	Thursday, March 13, 2008	**SPRING 2008**

You should write your results on the exam sheets only. Partial credit will be given only if you show your work and reasoning clearly.

Name: _____

SID: _____

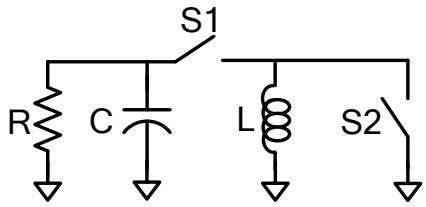
Problem 1 _____/ 15

Problem 2 _____/ 21

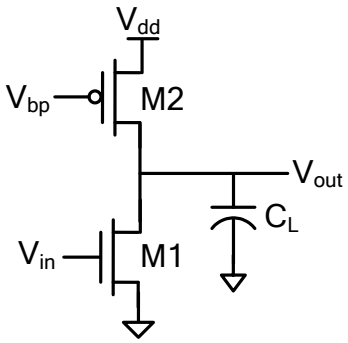
Total _____/ 36

Problem 1 (15 points) Noise and Swing

a) **(4 pts)** For the circuit shown below, assume that switch S1 is initially on and that switch S2 is initially off. When S1 is then turned off and S2 is turned on, what is the variance of the noise *current* that flows through S2 (i.e., the current that is sampled onto the inductor)? You can assume that the switches are ideal.



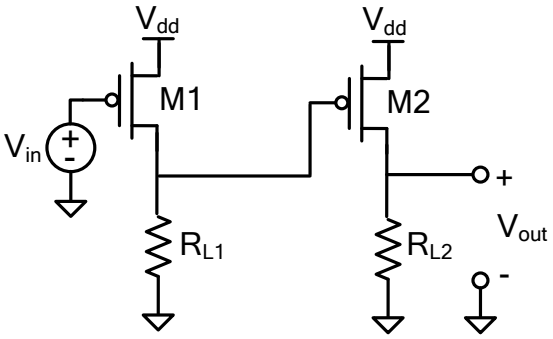
b) **(3 pts)** For the NMOS common-source amplifier shown below, what is the maximum swing allowed at the output? You can assume that the transistors require a minimum $|V_{ds}|$ of kV* (where $k \geq 1$) to meet the minimum required gain specification. You should provide your answer in terms of k, V1*, V2*, and V_{dd}.



c) **(8 pts)** Assuming V1* is fixed, how should V2* be chosen in order to maximize the achievable SNR at the output of the amplifier from part b)? You should give your answer as a function of k, V1*, and V_{dd}. Note that the majority of the credit for this problem will be given for showing the procedure you would follow to arrive at the final result.

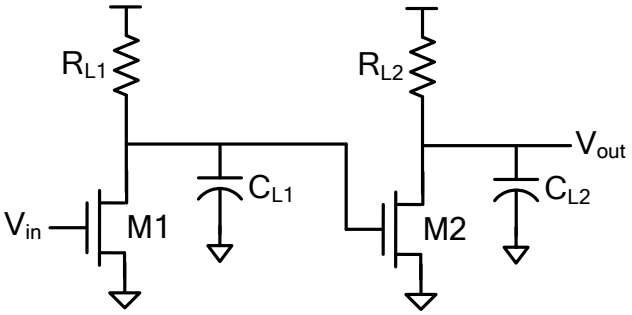
Problem 2 (21 points) Amplifier Design

a) **(4 pts)** What is the PSRR of the two-stage amplifier shown below? Note that PSRR for a single-ended amplifier is defined as $|(dV_{out}/dV_{in})|/|(dV_{out}/dV_{dd})|$. Please also take note that V_{in}, V_{out}, and V_{dd} are all referenced to ground. You can neglect the r_o of the transistors and all capacitors for this analysis.



b) **(5 pts)** Your co-worker Pat says that she can fix the PSRR problem with the design from part a) by changing just one of the two common-source stages and without using differential amplifiers. Is Pat right? If so, which stage would you change, and how would you change it? If not, why not?

c) **(6 pts)** What is the total noise at the output of the cascade of two common-source amplifiers shown below? You can ignore flicker noise, the r_o of the transistors, and all capacitors except those explicitly drawn in the diagram. You should provide your answer in terms of kT, C_{L1}, C_{L2}, γ, $A_{v1} = g_{m1}R_{L1}$, and $A_{v2} = g_{m2}R_{L2}$.



d) **(6 pts)** Now let's see what happens if we have a fixed total power budget that we are allowed to spend on the two stages of this amplifier and we would like to minimize the total noise contribution at the output. To simplify the analysis, you can ignore continue to ignore any parasitic capacitors from the transistors, and we will assume that the V*'s, gains, and bandwidths of the two stages are identical – i.e., $V1^* = V2^* = V^*$, $A_{v1} = A_{v2} = A_v$, and $R_{L1}C_{L1} = R_{L2}C_{L2} = \tau$. Finally, you should also assume that under these conditions, your answer to part c) would reduce to $v_{on}^2 = \frac{kT}{C_{L1}} \frac{1}{2} A_v^3 + \frac{kT}{C_{L2}} A_v$.

With these assumptions, what portion *k* of the total power would you allocate to M1 in order to minimize the total noise at the output? (Hint: In order to maintain a fixed gain-bandwidth, the power consumption of each stage is linearly proportional to its load capacitance.)