EECS40, FALL/2001
MIDTERM #2
Professor Oldham

- Closed book and notes except 1 page of formulas.
- You may use a calculator.
- Do not unstaple the exam.
- Show all your work and reasoning on the exam in order to recieve full or partial credit.
- This exam contains 6 problems and corresponding worksheets plus the cover page.
- Do not ask questions during the exam. If you believe there is an error, please point it out. If you believe there is an ambiguity, explain your interpretation in your answer.

NMOS Equations: if VDS>VDSSAT
ID = IDS (1 + lambda VDS)

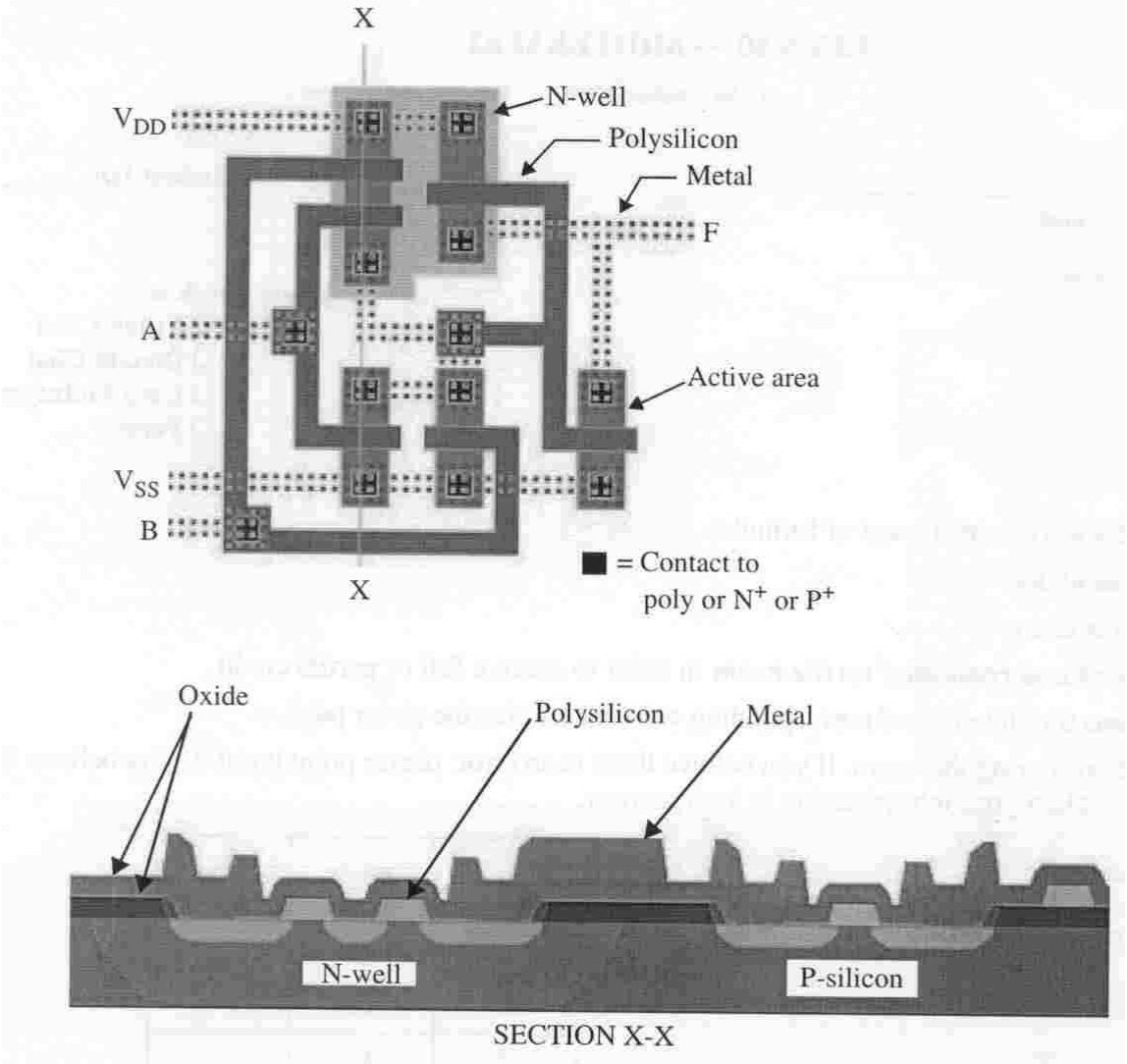
ID = kVS W/L (VGS-VT)

Problem	Points Possible	Your Score
1	15	
2	10	
3	15	
4	20	
5	20	
6	20	
Total	100	

$f = 10^{-15}$
$p = 10^{-12}$
$n = 10^{-9}$
$\mu = 10^{-6}$
$m = 10^{-3}$
$K = 10^{3}$
$M = 10^{6}$

Problem #1

Shown below is the layout of a CMOS circuit. The mask boundaries are indicated in a few places. The connection to ground (VSS),(VDD), the output F, and the two inputs A and B are identified on the layout. A cross section through X-X is also shown below, and the materials are identified.

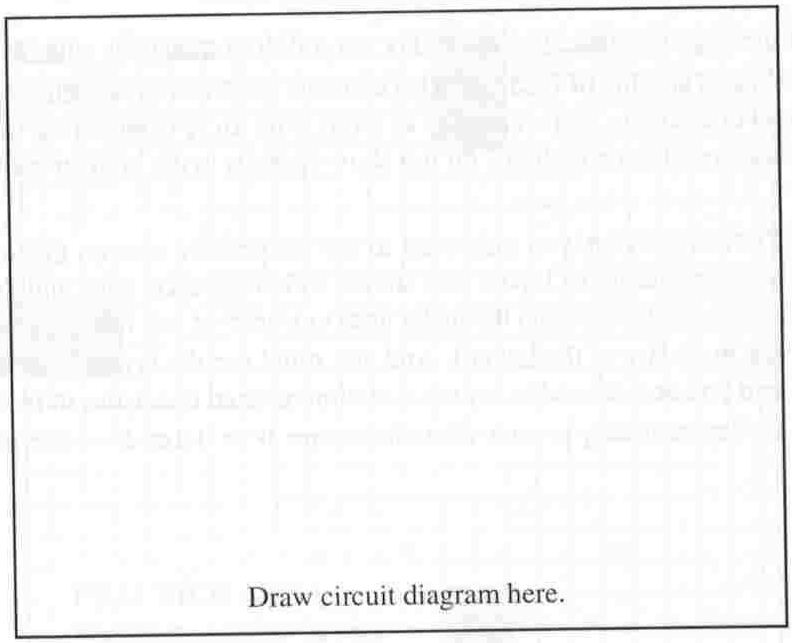


(a)Draw the circuit diagram and rearrange it to be a reasonably neat drawing. Obviously, the drawing should contain only NMOS and PMOS transistors and wires. You must, of course, label the inputs, outputs, and power supply connections.

(b)Write the truth table for the logic circuit. (Voltage of VDD means logical 1.)

Problem 1 Answer sheet

(a)



(b)

A	B		F

Truth Table

Problem #2

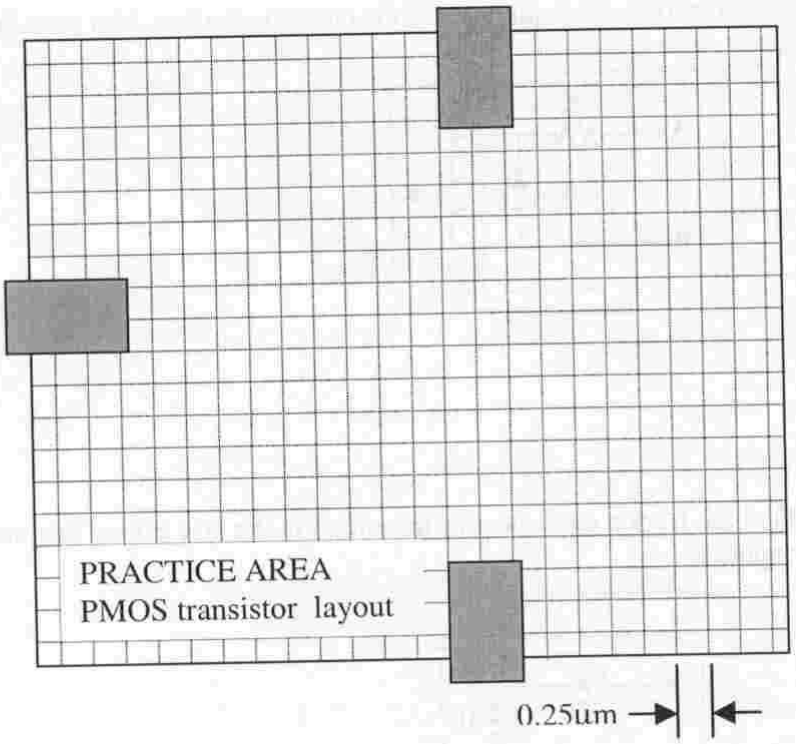
On the page opposite, you are to lay out a PMOS transistor with W=1um, L=0.25um. Note that a grid is provided with a grid spacing of 0.25um. Aslo note that the drawing conventions are shown; you must use these symbols in your layout. (For example, draw contacts as a box with an X from corner to corner, and draw the polysilicon mask with simple dashed lines.) For simplicity, do not show contacts to the body or well and do not show the location of the select masks.

(a) Draw the layout- you may want to use the practice area on the top of the sheet- it will be ignored. But you must put your answer in the layout area shown with the source, gate,drain connected to the metal lines shown. You will, of course, want to extend the metal lines to wherever you make contacts(we have just defined where the metal lines are at the boundary of the layout) and you must use the layout symbols indicated. The minimum feature size is 0.25um, and you do not need to lay out a minimum-sized transistor; in fact, it is better to make things a bit "looser" just so that the layout is easy to read. (But, do be sure W=1um, L=0.25um)

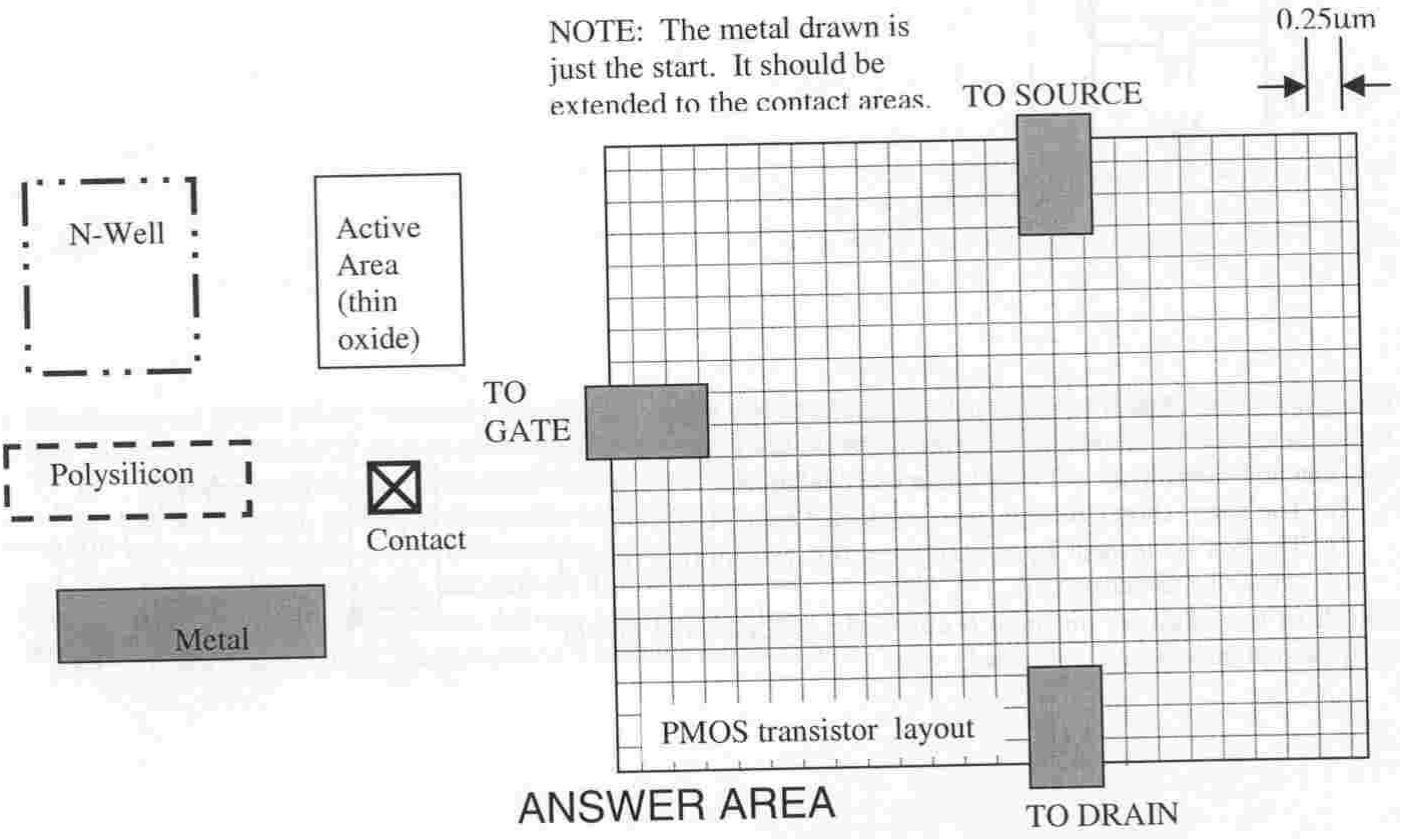
(b)Indicate here the polarity of the masks (dark or clear field)
Well mask ---------- field
Active area mask ---------- field
Polysilicon mask ---------- field
Contact mask ---------- field
Metal mask ---------- field

Problem 2 Answer sheet
(a)

USE THIS AREA FOR ROUGH LAYOUT, BUT PUT ANSWER IN LAYOUT BOX BELOW

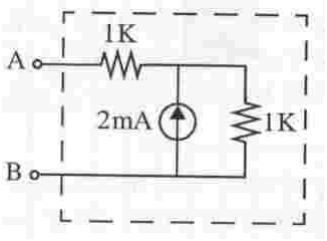


(b)

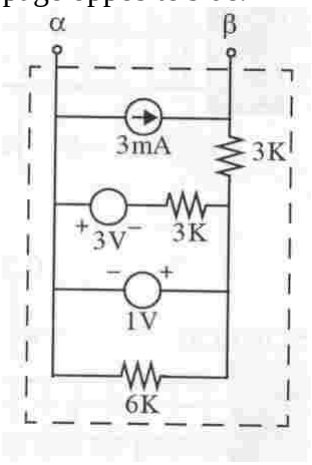


Problem #3

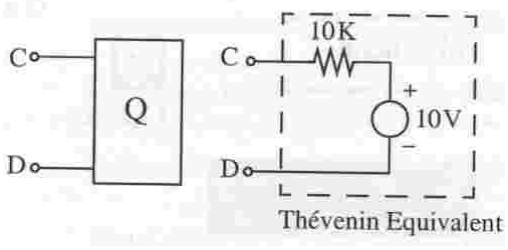
(a)Find the thevenin equivalent of the circuit in the box. you must draw it in the answer box provided on the page opposite side.



(b)Find the norton equivalent of the circuit in the box. you must draw it in the answer box provided on the page opposite side.

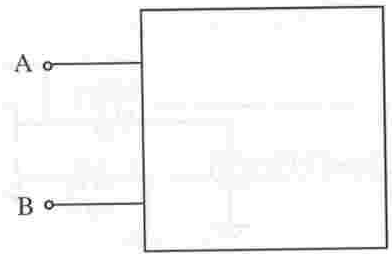


(c)Through a series of tests you find that the circuit in the box Q has thevenin equivalent shown, but you really do not know what is in the box. You now consider power flow under two conditions:
1) The box is short circuited (wire connected across C-D) 2) The box is loaded by connecting a 10k resistor ("load") across terminals C-D.
Which of the answers on page 6 correctly describe the power dissipation in the box and in the load?

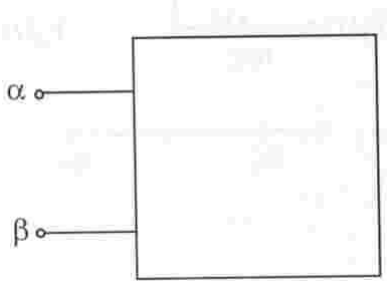


Problem 3 Work and Answer sheet

(a)



(b)

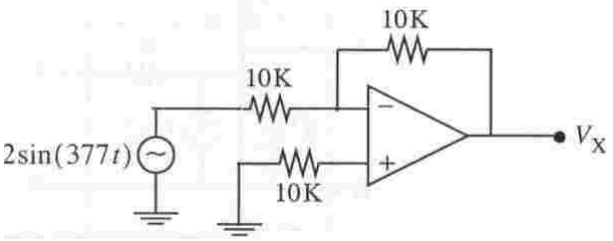


(c)Which answers below (if any) correctly describe the power dissipated within the box and the power dissipated in the load (short or 10k resistor)? Any number from zero to all 6 may be correct. Circle correct statements.

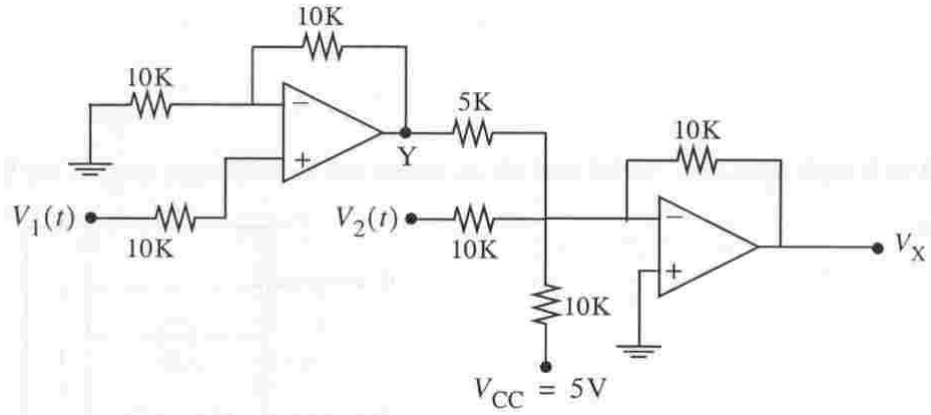
1) when shorted the power dissipation in the box is a minimum.
2) when shorted the power dissipation in the box is a maximum.
3) when shorted the power delivered by the box is zero.
4) when loaded (10k) the box delivers 10mW to the load.
5) when loaded (10k) the box delivers 2.5mW to the load.
6) when loaded (10k) the dissipation within the box is 2.5mW.

Problem #4

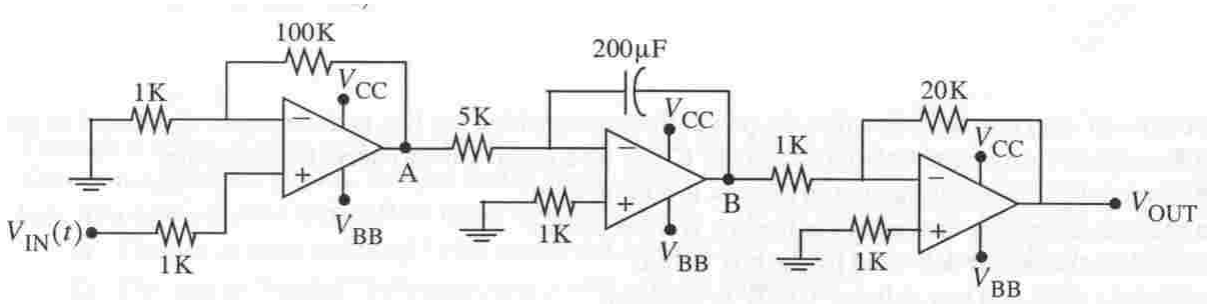
Find the unknown voltages for the following two op-amp circuits using the ideal op-amp model.
(a)

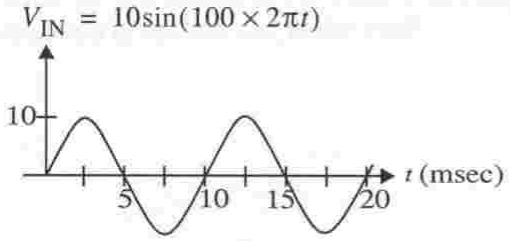


(b)



(c)Now consider the op-amp circuit below, that is powered by a positive supply VCC of +5V and a negative supply VBB of -5V (resulting in rails of +5V and -5V). Given the input waveform shown, neatly sketchthe waveforms at the nodes A, B, OUT. Be sure to choose the vertical scales on the plots so that the curves are easily read. You cannot change the horizontal (time axis) scales; that is given. Note: Label the voltage axis in all cases (they may be different for the three different answers).



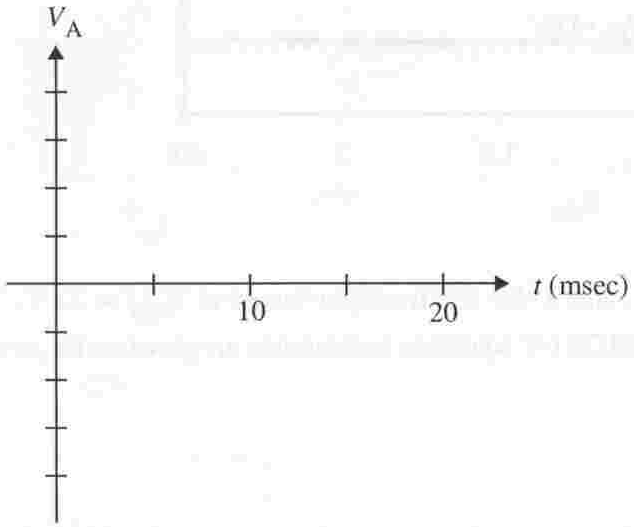


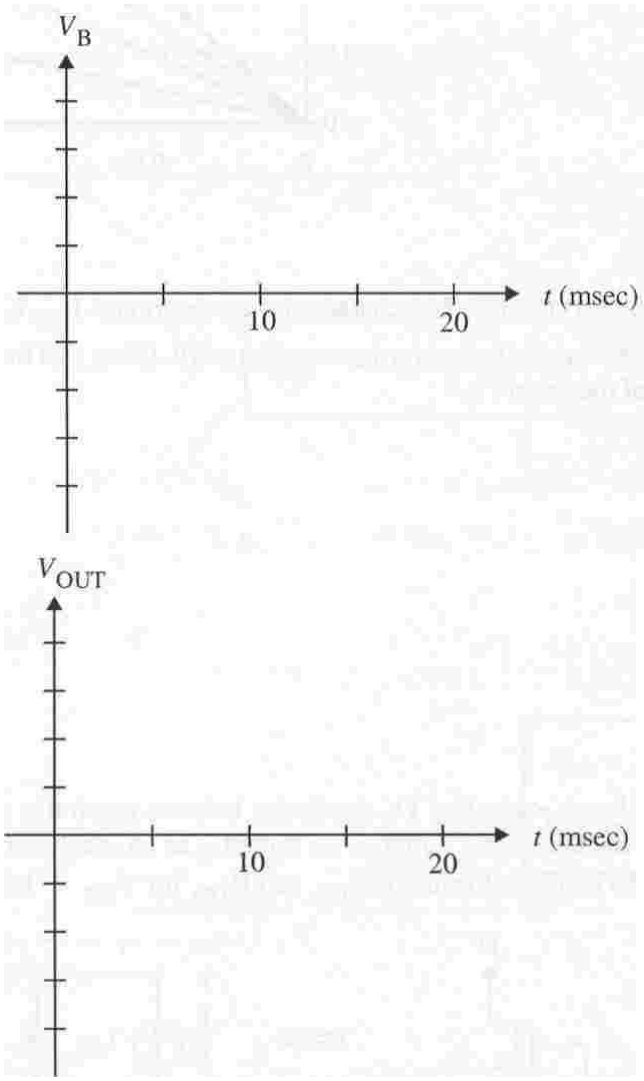
Problem 4 Answer sheet

(a) VX = ----------

(b) VY = ---------- VX = ----------

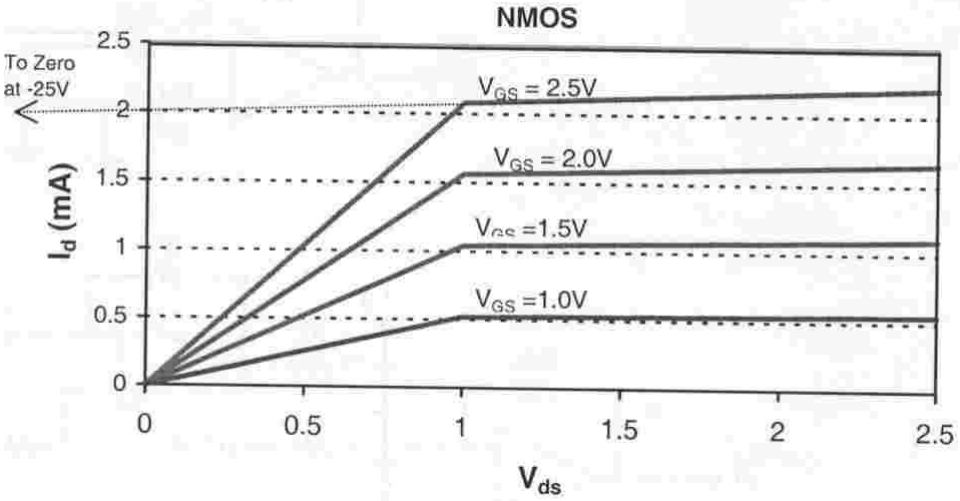
(c)




V_B
t (msec)
10
20
V_{OUT}
t (msec)
10
20

Problem #5

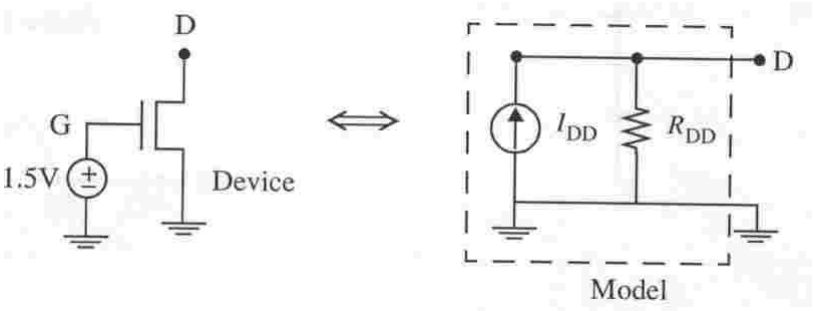
Consider the NMOS transistor whose I versus V characteristics are shown in the figure below. This is a device with W=2um, L=0.2um. Note that the straight line portion of the I-V curve, when extrapolated to the voltage axis, intersects at -25V. Note also the we determine the threshold voltage to be approximately 0.5V from these characteristics.



(a) Based on these I-V characteristcs, determine IDS, kVS and Lambda for this transistor biased at VGS=2.5V. Put the answers in the answer boxes on page 10. (Note that the NMOS I-V equations in saturation are given on the coversheet of the exam.)

(b) If VDS=2.5V, what values of VGS would be required to achieve a drain current of exactly 1mA?

(c) We note that for drain voltages exceeding 1V, the device behaves much like a current source (actually, a "sink" since the current is going into the drain). So suppose we model it as an ideal current source in parallel with a resistor, as shown below. What are the numerical values of IDD and RDD for VGS=1.5V?



Problem 5 Answer sheet

(a)

IDS = ---------- units?

kVS = ---------- units?

Lambda = ---------- units?

(b) VGS = ---------- units?

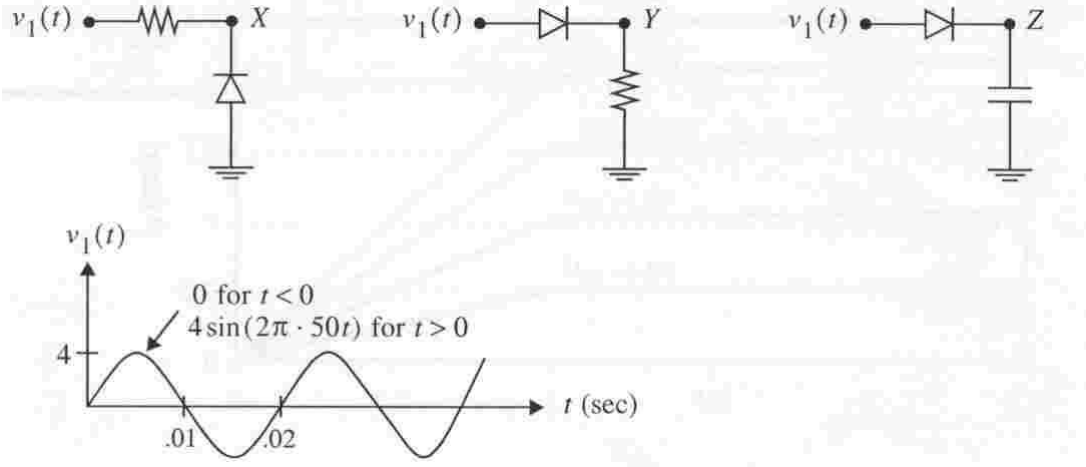
(c)

IDD = ---------- units?

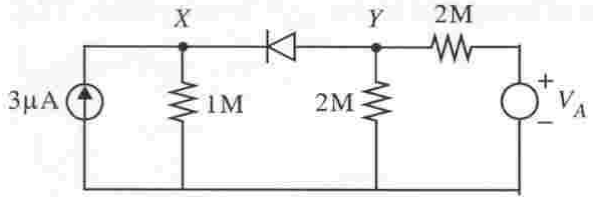
RDD = ---------- units?

Problem #6

(a)Three circuits are shown below as well as the input waveform that drives each one. Carefully sketch VX(t), VY(t) and VZ(t) on the axes provided on the answer page, opposite. Treat all components as ideal (including the diode that acts like a prefect rectifier.)

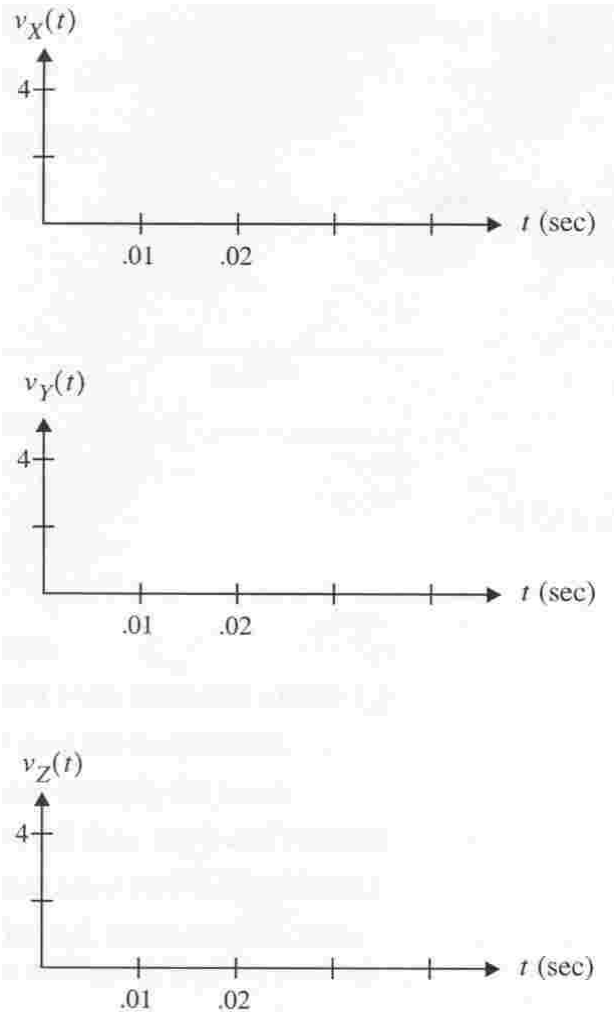


(b)The source VA in the circuit below is adjustable from -5V to +10V. Neatly sketch VX and VY on the axes provided on page 12 as a function of VA. The sketch should cover the full range of VA from -5 to +10V. Again , you may assume the diode is a perfect rectifier.



Problem 6 Answer sheet

(a)



(b)