UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Oldham

Fall 1999

EECS 40 — FINAL EXAM

13 December 1999

Name: Solutions
Last, First

Student ID: _____

TA: ❑ Kusuma
❑ Chang

Guidelines:

(a) One page of notes allowed (both sides).

(b) You may use a calculator.

(c) Do not unstaple the exam.

(d) Show ***all your work and reasoning on the exam*** in order to receive full or partial credit.

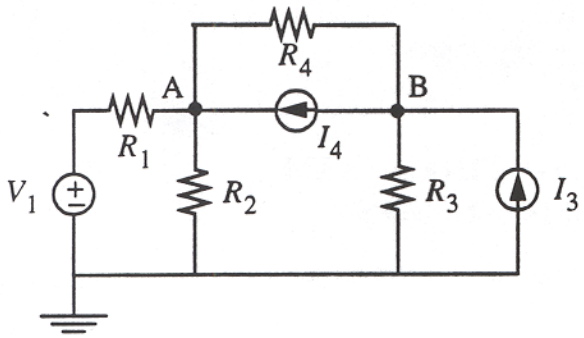
(e) This exam contains 16 pages plus the cover page and 2 sheets of scratch paper included at the end of the exam. You can remove these from the rest of the exam if you wish.

Problem	Points Possible	Your Score
1	20	
2	25	
3.	30	
4	25	
5	25	
6	20	
7	25	
8	30	
Total	**200**	

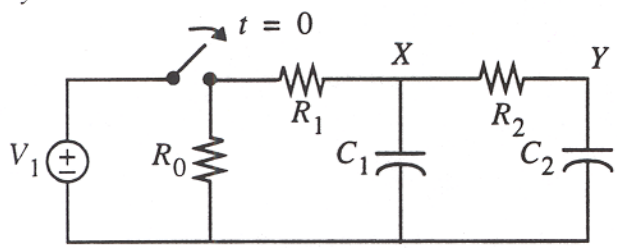
$K = 10^3$
$m = 10^{-3}$
$\mu = 10^{-6}$
$n = 10^{-9}$
$p = 10^{-12}$
$f = 10^{-15}$

Problem 1 Nodal Analysis (20 points)

(a) Write 2 nodal equations sufficient to find voltages A and B.



(b) The switch closes at $t = 0$ (after a very long time open). Write 2 nodal differential equations describing V_x and V_y.



$I_{C_1} = C_1 \frac{dV_x}{dt}$

$I_{C_2} = C_2 \frac{dV_y}{dt}$

(c) What are the values of V_x, V_y at $t = 0^+$ and $t \to \infty$?

Before switch is closed, no voltage across C_1 and C_2.
We know voltage across a capacitor is continuous.
$\therefore V_x(t=0^+) = V_y(t=0^+) = 0\ V.$

As $t \to \infty$, no current flows thru C_1 and C_2
$\therefore V_x(t \to \infty) = V_y(t \to \infty) = V_1$

Problem 1 Answers

(a)

$$\frac{V_A - V_1}{R_1} + \frac{V_A}{R_2} + \frac{V_A - V_B}{R_4} - I_4 = 0$$

$$I_4 + \frac{V_B - V_A}{R_4} + \frac{V_B}{R_3} - I_3 = 0$$

(b)

$$\frac{V_x - V_1}{R_1} + C_1 \frac{dV_x}{dt} + \frac{V_x - V_y}{R_2} = 0$$

$$\frac{V_y - V_x}{R_2} + C_2 \frac{dV_y}{dt} = 0$$

(c)

$V_x(t = 0^+) =$ 0 V

$V_y(t = 0^+) =$ 0 V

$V_x(t \to \infty) =$ V_1

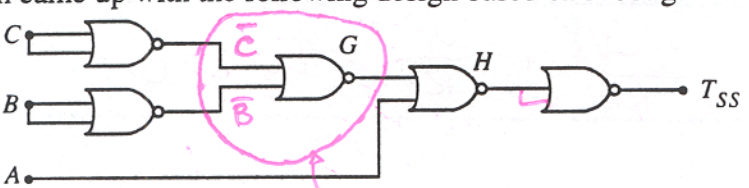
$V_y(t \to \infty) =$ V_1

Problem 2 Nerd Contest (25 points)

In a post-Big Game Nerd Competition, teams from Stanford and UCB were asked to draw logic diagrams to implement the following function:

$$T = A + BC$$

The Stanford team came up with the following design based on NOR gates



Design SS

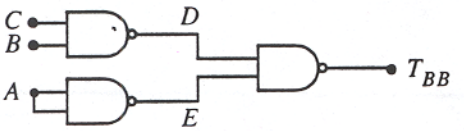
see below

$G = CB$

$H = \overline{G+A}$

$T_{SS} = \overline{H}$

The Berkeley team came up with the following design based on NAND gates:



Design BB

$D = \overline{CB}$

$E = \overline{A}$

$T_{BB} = \overline{DE}$

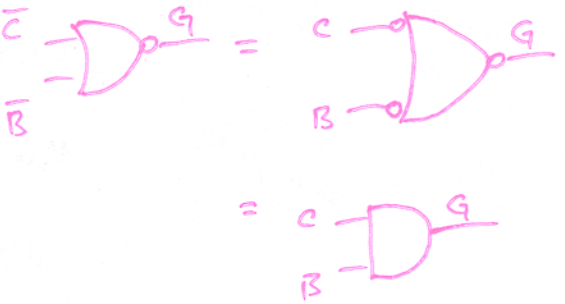
(a) Fill out the truth tables opposite to evaluate T_{SS} and T_{BB}.

(b) Do both circuits function as desired?

(c) Define the unit gate delay of the NOR gates as τ_{NOR} and unit gate delay of the NAND as τ_{NAND}. Assume the outputs, T, are loaded by similar gates. What is the delay of the Stanford circuit and what is the delay of the Berkeley circuit (in terms of τ_{NOR}, τ_{NAND})?

When you tie together the inputs of a NOR gate, (A = B) it behaves like an inverter.

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0



$\Rightarrow G = CB$

$H = \overline{G+A}$

Problem 2 Worksheet and Answers

(a)

FILL OUT WITH ZEROS AND ONES

A	B	C	G	H	T_{SS}	D	E	T_{BB}
0	0	0	0	1	0	1	1	0
0	0	1	0	1	0	1	1	0
0	1	0	0	1	0	1	1	0
0	1	1	1	0	1	0	1	1
1	0	0	0	0	1	1	0	1
1	0	1	0	0	1	1	0	1
1	1	0	0	0	1	1	0	1
1	1	1	1	0	1	0	0	1

both correctly implement $A + BC$

(b)

Function correct? (yes or no?)

T_{SS} YES

T_{BB} YES

(c) Delay

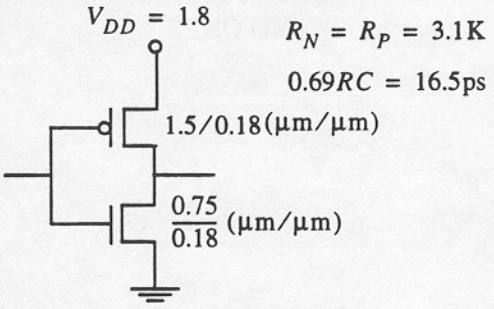
SS Circuit 4 T_{NOR}

BB Circuit 2 T_{NAND}

Problem 3 Nerd Contest – Details (30 points) (Independent of Problem 2)

(a) The schematic of a CMOS inverter analyzed in Lecture 25 is shown in the figure below. Note the unit gate delay is 16.5 ps when the inverter drives an identical inverter.

Using the same CMOS technology, you are to design (that means draw the schematic of) a 2-input NAND gate [NOT a layout please!]. Please size the devices for equal worst-case rise and fall times, and use 1.5/0.18 as the p-channel device size.



(b) Find the input capacitance and the output resistance of such a NAND gate (worst case). Compute the gate delay assuming the NAND gate drives the inputs to identical NAND gates. Ignore drain-bulk and interconnect capacitance.

(c) Now draw the schematic of the NOR gate and indicate device sizes needed to get equal (worst-case) rise and fall times. Again use 1.5/0.18 as the p-channel device size.

(d) Find the input capacitance and the output resistance of such a NOR gate. Compute the unit gate delay assuming the NOR gate drives the inputs to identical NOR gates. Ignore drain-bulk and interconnect capacitance.

For the inverter in the figure above,

$16.5ps = 0.69RC \Rightarrow C = (C_{GP}+C_{GN}) = 16.5ps / (0.69 \cdot 3.1k\Omega)$

$C = 7.71fF$, $C \propto$ Area

Area(PMOS) = 2 Area(NMOS)

$\therefore C_{GN} = 7.71fF \times \frac{1}{3} = 2.57fF$ ($0.75\mu m \times 0.18\mu m$)

$C_{GP} = 7.71fF \times \frac{2}{3} = 5.14fF$ ($1.5\mu m \times 0.18\mu m$)

(b) $C_{GN} = 5.14fF$

$C_{GP} = 5.14fF$ (∵ Both have W/L = 1.5/0.18)

$R = 3.1k\Omega$

$\tau = 0.69 \times R \times (C_{GN}+C_{GP}) = 22psec$

(d) $C_{GN} = 1.29fF$ ($0.375\mu m \times 0.18\mu m = \frac{1}{4} \times 1.5\mu m \times 0.18\mu m$)

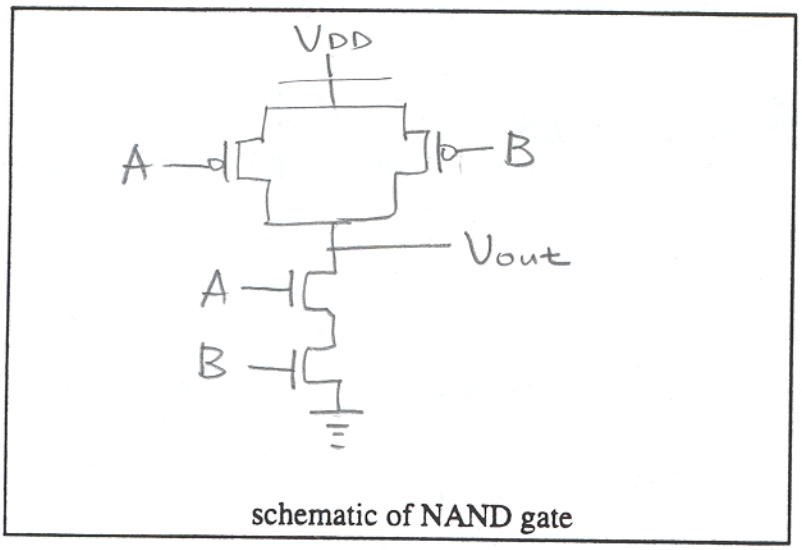
$C_{GP} = 5.14fF$

$R = 6.2k\Omega$

$\tau = 0.69 \times R \times (C_{GN}+C_{GP}) = 27.5psec$

Problem 3 Worksheet and Answers

(a)



schematic of NAND gate

PMOS $\frac{W}{L} = \frac{1.5}{0.18}$

NMOS $\frac{W}{L} = \frac{1.5}{0.18}$

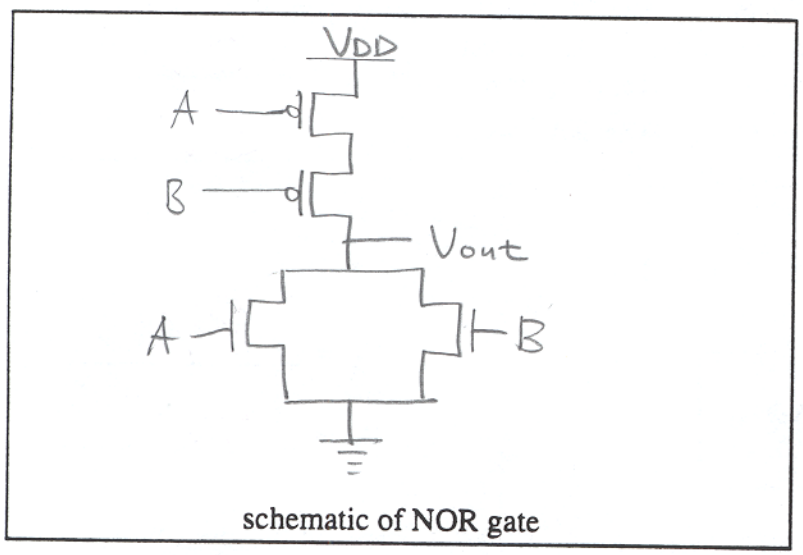
$1 R_P = 2 R_N$

$\therefore$ NMOS $\frac{W}{L} = \frac{1.5}{0.18}$

(b) C_{GP} = 5.14 fF C_{GN} = 5.14 fF

R = 3.1 K Unit Gate Delay = 22 pS

(c)



schematic of NOR gate

PMOS $\frac{W}{L} = \frac{1.5}{0.18}$

NMOS $\frac{W}{L} = \frac{0.375}{0.18}$

$2 R_P = 1 R_N$

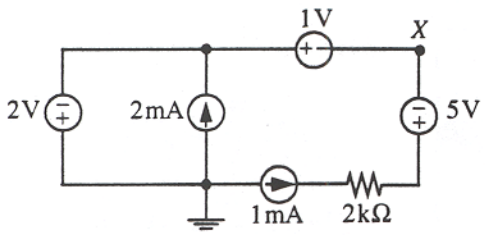
$\therefore$ NMOS $\frac{W}{L} = \frac{0.375}{0.18}$

(d) C_{GP} = 5.14 fF C_{GN} = 1.29 fF

R = 6.2 K Unit Gate Delay = 27.5 pS

Problem 4 Simple Circuits (25 points)

(a)

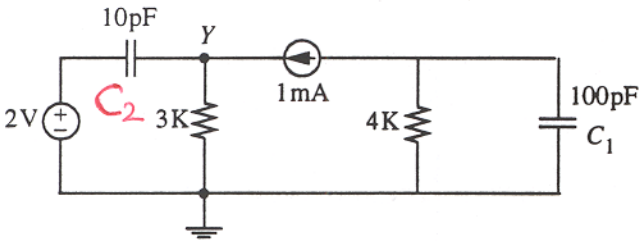


V_X = -3V

Power delivered by 1mA source = 4mW

Power delivered by 2mA source = -4mW

(b)

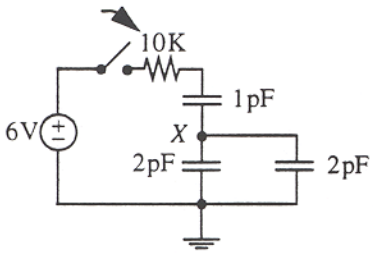


V_Y = 3V

Power delivered by 1mA source = 7mW

Energy stored in C_2 = 5pJ

(c)

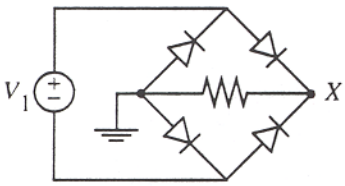


Capacitors are initially uncharged. Find V_X long after the switch is closed. Find peak power P_{MAX} delivered by the voltage source.

V_X = $\frac{6}{5}$V = 1.2V

P_{MAX} = 3.6mW

(d)

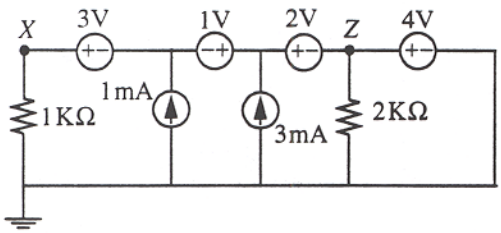


Assume the 4 diodes are perfect rectifiers. (a) What is V_X when V_1 = 5V ? (b) What is V_X when V_1 = -5V ?

a) V_X = 5V

b) V_X = 5V

(e)

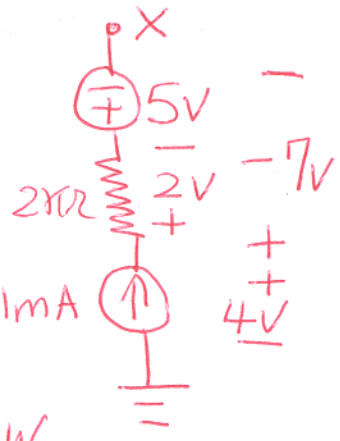


V_X = 8V

V_Z = 4V

Problem 4 Worksheet

$V_X = -2 - 1 = -3V$

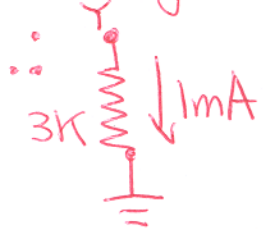


1mA source (delivered): $(1mA)(4V) = 4mW$

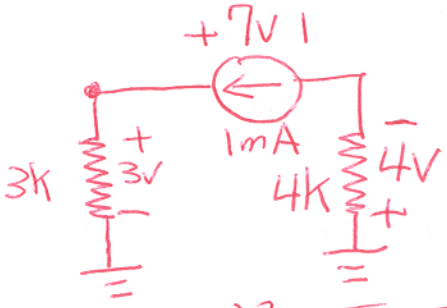
2mA source (delivered)

$\Rightarrow (2mA)(-2V) = -4mW$

At steady-state, capacitor acts like open circuit.



$V_Y = (1mA)(3k) = 3V$



$Power = (7V)(1mA) = 7mW$

Voltage across C_2 = $2V - V_Y = -1V$

$E_{C_2} = \frac{1}{2}CV^2 = \frac{1}{2}(10pF)(-1)^2 = 5pJ$

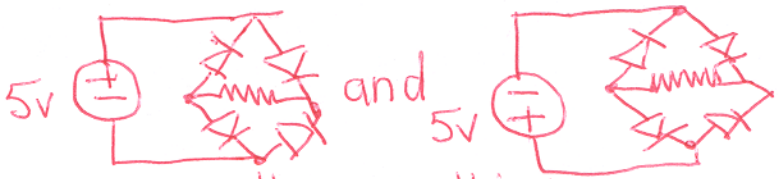
By capacitor-voltage division, $V_X = 6v\left(\frac{1pF}{1pF+4pF}\right) = \frac{6}{5} = 1.2V$

Get peak power when capacitors act like short circuits, so

$P_{max} = \frac{V^2}{R} = \frac{(36)}{10k} = 3.6mW$

$V_X = 5V$ for part (a)

$V_X = 5V$ for part (b) because



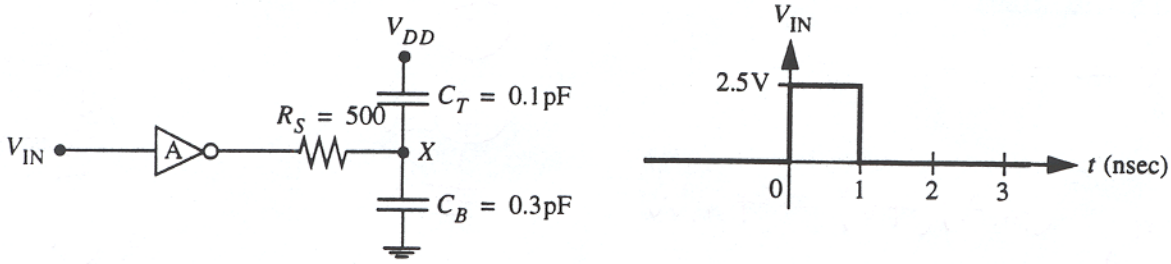
are the same thing!

$V_Z = 4V$

$V_X = 3V - 1V + 2V + 4V = 8V$

(you shouldn't have done nodal analysis)

Problem 5 Inverter Transient (25 points) Solutions



Inverter A is a CMOS inverter with effective output resistance of 1.5K. V_{DD} = 2.5V and V_{Tl} = 0.7, V_{Th} = 1.8V.

The input capacitance is 5 fF, V_{IN} was zero for $t<0$, then a pulse generator (with very low output resistance) produces the input waveform shown above.

(a) Sketch the general form of $V_{OUT}(t)$.

(b) Calculate V_{OUT} at t = 0+, t = 1 nsec, and t = 2 nsec.

(c) Re-sketch $V_{OUT}(+)$ very carefully and neatly.

$\tau = RC = (1.5k + .5k)(.3p + .1p)s$

$= .8ns$

$V_{out}(0) = 2.5e^{-0/.8} = 2.5V$

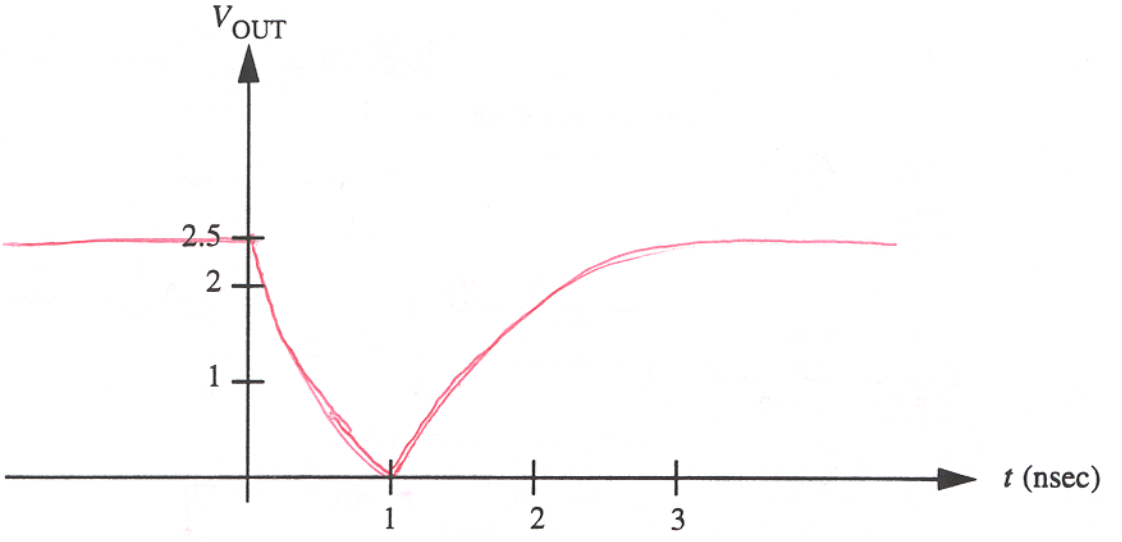
$V_{out}(1) = 2.5e^{-1/.8} = .716V$

$V_{out}(2) = 2.5 + -(.72 - 2.5)e^{-(2-1)/.8}$

Solutions

Problem 5 Answer Sheet

(a)



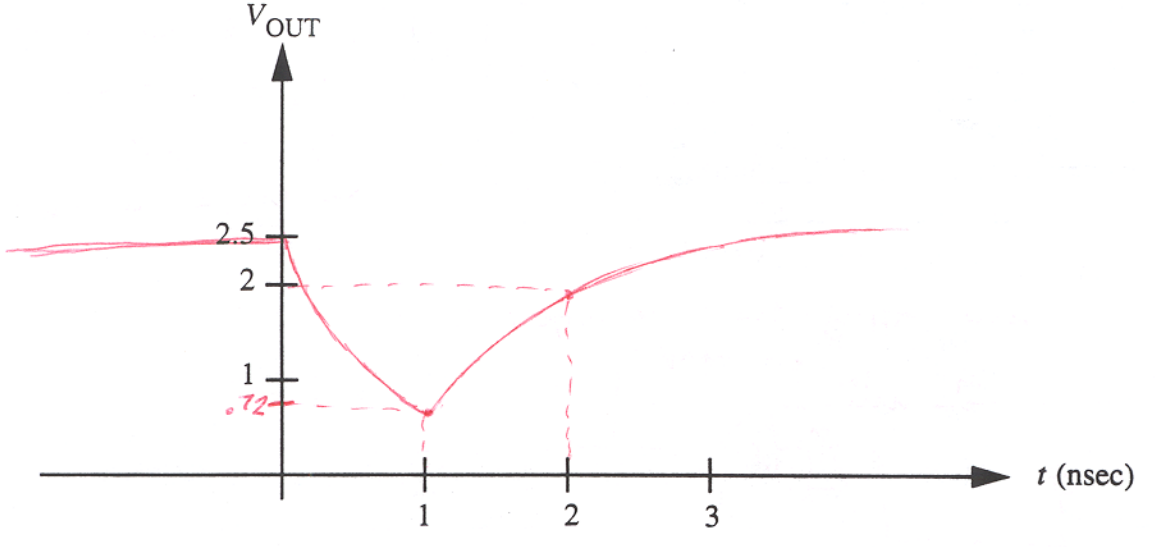
(b)

b.1) $V_{OUT}(t = 0+)$ = 2.5V

b.2) $V_{OUT}(t = 1 \text{ nsec})$ = .72V

b.3) $V_{OUT}(t = 2 \text{ nsec})$ = 1.99V

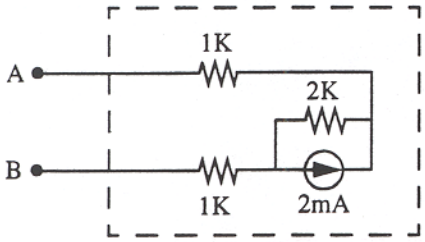
(c)



Problem 6 Thévenin Equivalents (20 points)

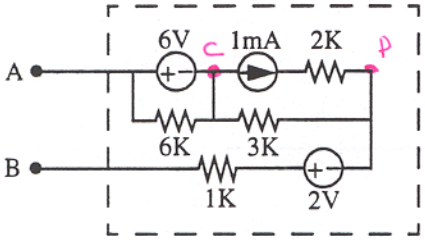
Find the Thévenin equivalent circuit for each of the following.

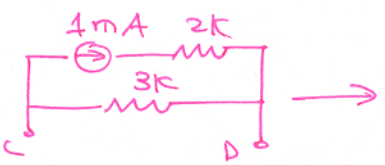
(a)

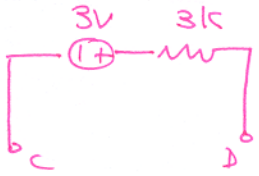


source transformation :

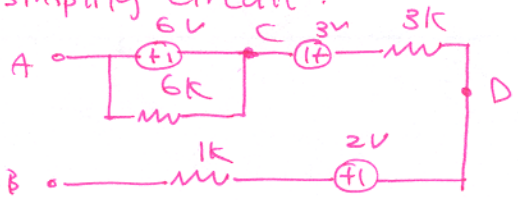
(b)



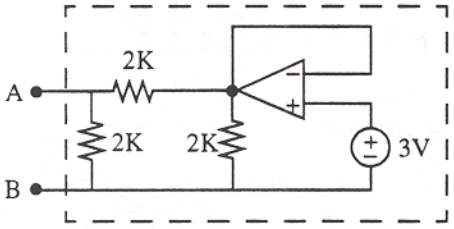




simplify circuit :

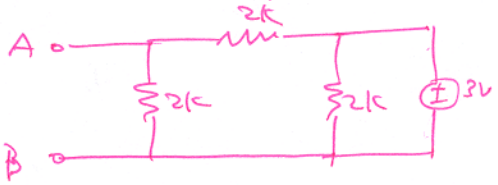


(c)

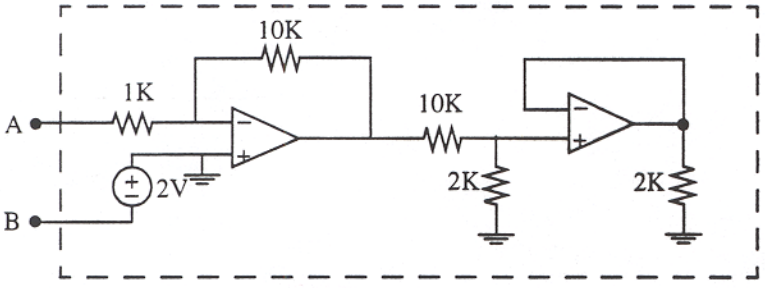


(Op-amp is ideal)

output of op-amp always 3V :



(d)



(Op-amps are ideal)

$V_+ = V_- = 0V$.

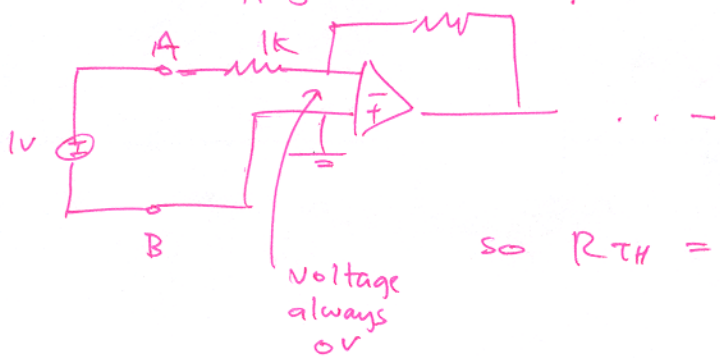
if AB open circuit

$V_A = V_- = 0V$

$V_B = -2V$

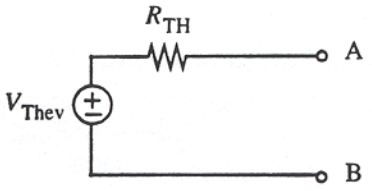
so $V_{TH} = V_A - V_B = 2V$

now apply test voltage :



so $R_{TH} = 1k\Omega$

Problem 6 Worksheet and Answers



(a)

V_{TH} = 4K

R_{TH} = 4V

(b)

V_{TH} = 4K

R_{TH} = 1V

(c)

V_{TH} = 1.5V

R_{TH} = 1K

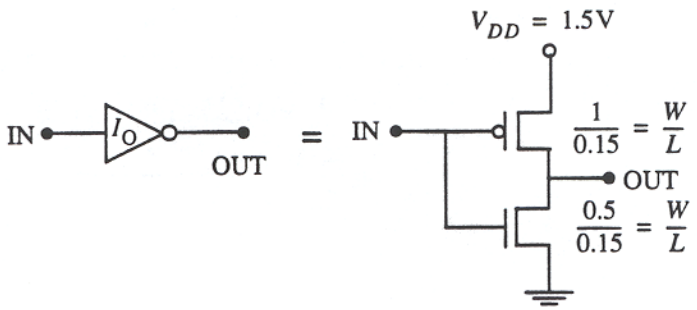
(d)

V_{TH} = 2V

R_{TH} = 1K

Problem 7 Capacitive Load (25 points)

We are designing a CMOS logic circuit with the latest devices that use $L = 0.15\mu m$. An inverter schematic is shown for the basic inverter

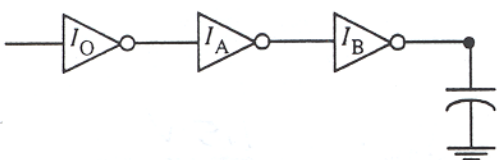


C_{Gp} = 2fF
C_{Gn} = 1fF
R_p = 3.5K
R_n = 3.5K

We need to drive an interconnect wire going across the chip with a capacitance of 192 fF.

(a) Estimate the stage delay (time to switch the output from zero to $V_{DD}/2$ with the input going from V_{DD} to 0) if this inverter drives the wire directly. The 192fF load is connected to the node labeled "OUT".

(b) Suppose we insert two "buffer inverters" that have larger W/L (and therefore, lower R_p, R_n) to drive the load capacitance faster:



For Inverter A: $\left.\frac{W}{L}\right|_N = \frac{2}{0.15}$, $\left.\frac{W}{L}\right|_P = \frac{4}{0.15}$ } ×4

For Inverter B: $\left.\frac{W}{L}\right|_N = \frac{8}{0.15}$, $\left.\frac{W}{L}\right|_P = \frac{16}{0.15}$ } ×16

Now we suffer 3 stage delays! But let's compute them – maybe it's not so bad. Assume the load on I_O is the gate capacitance of I_A and similarly that the load on I_A is the input capacitance of I_B.

(b.1) Compute C_{Gn} and C_{Gp} for I_A and I_B.

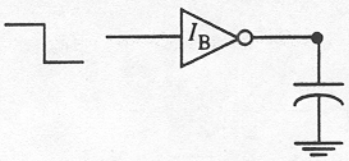
(b.2) Compute R_p and R_n for I_A and I_B.

(c-e) Find the unit gate delay for all 3 stages (input step $V_{DD} \rightarrow 0$ or 0 - V_{DD} and output moving from 0 to $V_{DD}/2$ or V_{DD} to $V_{DD}/2$).

(f) Compare total gate delay with that of part (a).

Problem 7 Worksheet and Answers

(a)



$0.69RC = .69 \times 3.5K \times 192 \times 10^{-15}$

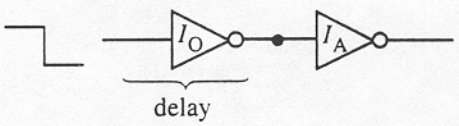
Unit gate delay = 464 ps

(b)

C ↑ x16 or 4
R ↓ x16 or 4

	Inverter A	Inverter B
C_{Gn}	4 fF	16 fF
C_{Gp}	8 "	32 "
R_p	875	219
R_n	875	219

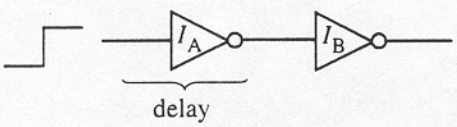
(c)



$.69RC = .69 \times 3.5K \times 12fF$

Unit gate delay = 29 ps

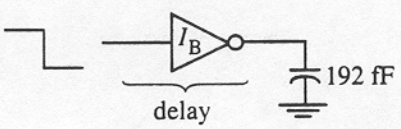
(d)



$.69RC = .69 \times 875 \times 48fF$

Unit gate delay = 29 ps

(e)



$.69RC = .69 \times 219 \times 192fF$

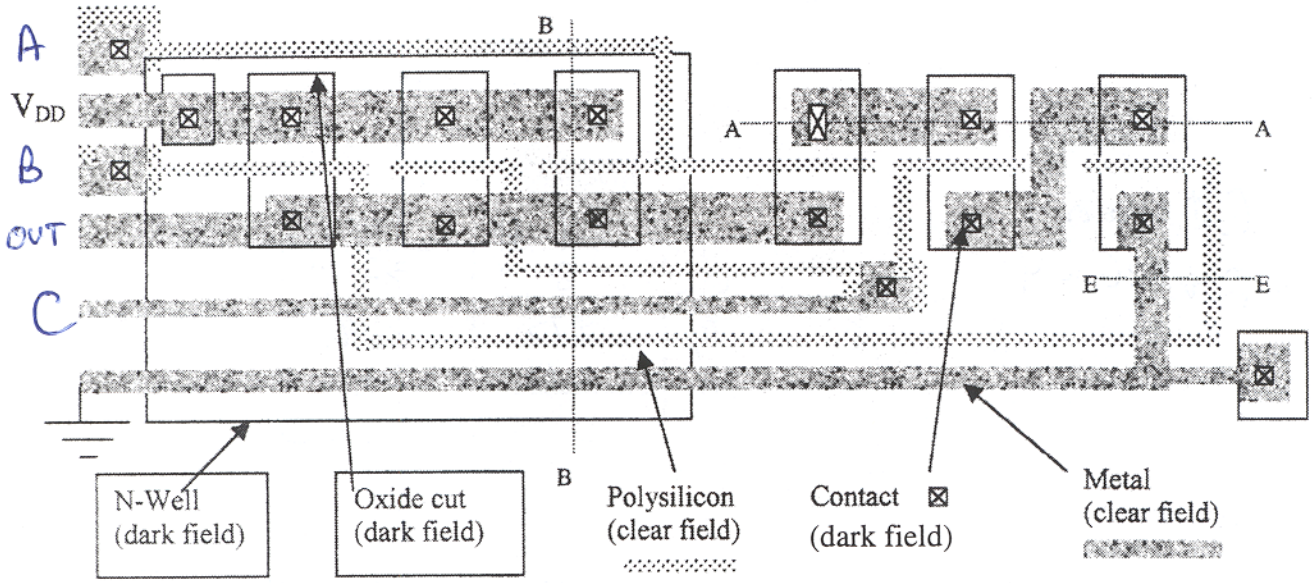
Unit gate delay = 29 ps

(f) Total of (c) + (d) + (e) 87 ps versus (a) 464 ps

3 delays << 1 delay !

Problem 8 CMOS Technology (30 points)

The layout of a CMOS logic circuit is shown below. Also shown on the page opposite is the cross-section E-E of the chip.



The CMOS process is:

(1) Start: p-Type Si wafer
(2) Well mask, implant donors
(3) Grow field oxide 0.5µm
(4) Pattern oxide (oxide cut for thin oxide)
(5) Grow gate oxide
(6) Deposit 0.5µm polysilicon
(7) Pattern polysilicon
(8) Two select masks with implants (masks not shown)
(9) Deposit 0.5µm oxide
(10) Contact mask, etch oxide
(11) Deposit 0.5µm metal
(12) Pattern metal

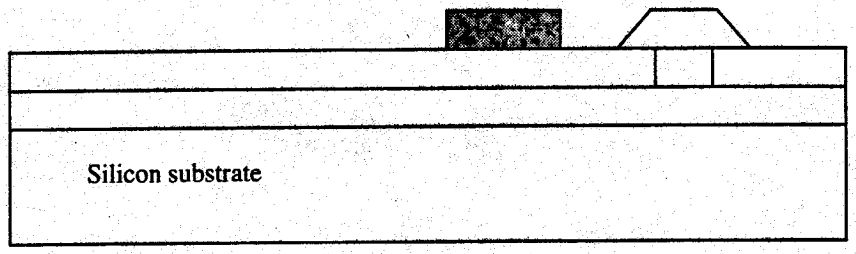
(a) In the space provided, draw cross-section A-A. Use E-E as a guide for scale.

(b) Draw cross-section B-B.

(c) Label the inputs and outputs of this circuit on the figure above. (Note that there are 6 wires entering from the left and of these, only 2 are labeled, namely V_{DD} and ground. You are to label the others and use these labels in part d.)

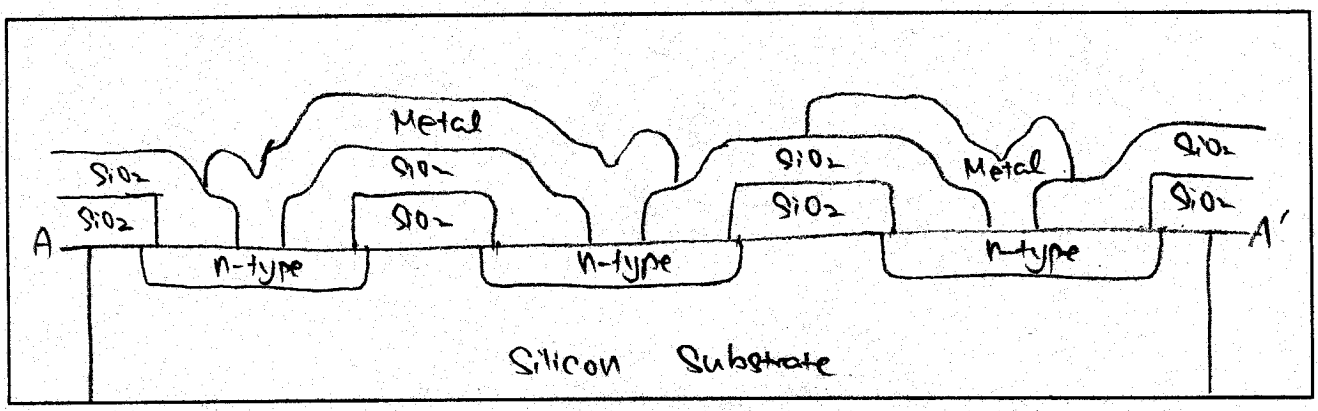
(d) Write the logic function of the circuit (for example, OUT = $\overline{(A+B)\cdot C}$).

Problem 8 Answers



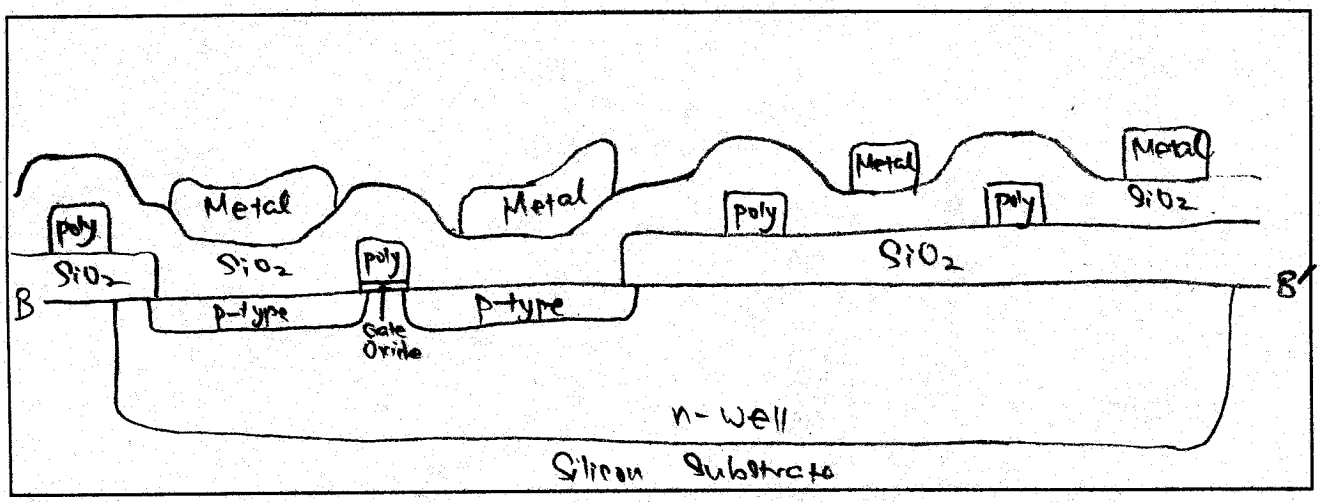
Cross-section E -- E

(a)



Cross-section A-A

(b)



Cross-section B-B

(c) (Label figure on opposite page.)

THANKS TO PAUL PARK!

(d) Logic Equation OUT = $\overline{A \cdot B \cdot C}$