UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Oldham

Fall 1999

EECS 40 — MIDTERM #2

10 November 1999

Name: _____
Last, First

Student ID: _____

TA: ❑ Kusuma
❑ Chang

Guidelines:

1. Closed book and notes except 1 page of formulas.
2. You may use a calculator.
3. Do not unstaple the exam.
4. Show ***all your work and reasoning on the exam*** in order to receive full or partial credit.
5. This exam contains 12 pages plus the cover page and 2 sheets of scratch paper included at the end of the exam. You can remove these from the rest of the exam if you wish.

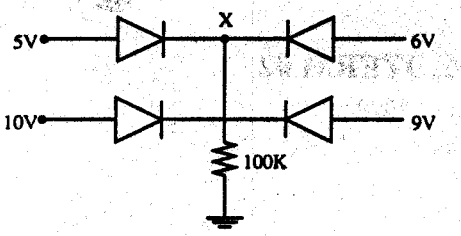
Problem	Points Possible	Your Score
1	20	
2	20	
3	20	
4	20	
5	20	
Total	**100**	

$K = 10^3$
$m = 10^{-3}$
$\mu = 10^{-6}$
$n = 10^{-9}$
$p = 10^{-12}$
$f = 10^{-15}$

Problem 1 (20 points)

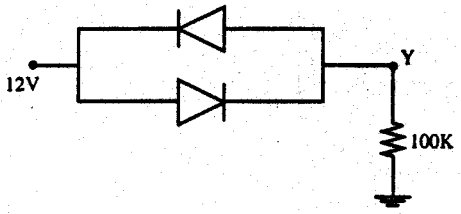
What is the value of the unknown node voltage in each of the following circuits? Assume diodes are perfect rectifiers.

(a) 2pts



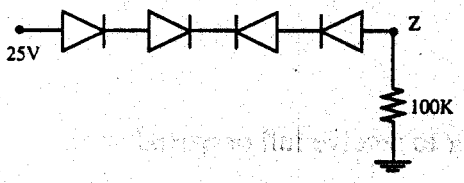
V_X = 10V

(b) 2pts



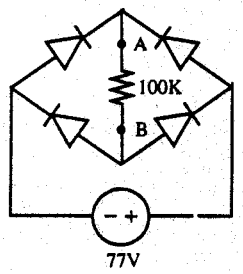
V_Y = 12V

(c) 2pts



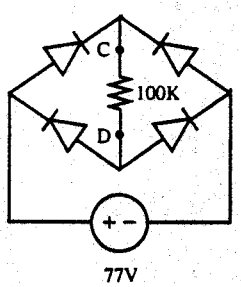
V_Z = 0V

(d) 3pts



V_{AB} = 77V

(e) 3pts



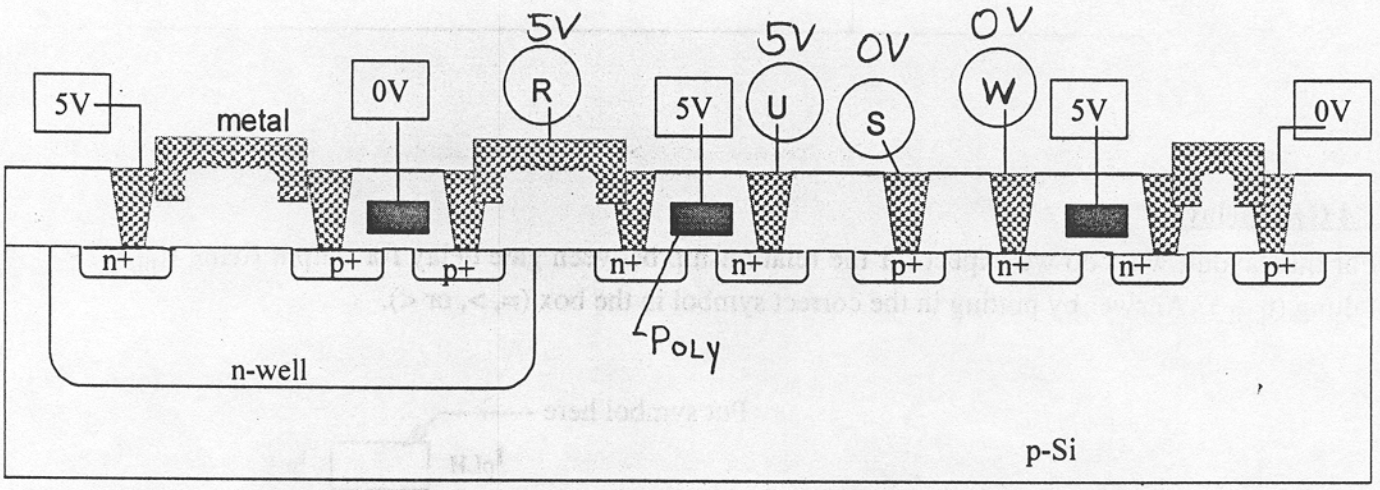
V_{CD} = 77V

(f) A cross-section for a CMOS chip is shown on the facing page. Some node voltages are indicated. Please tell us what the values are for the node voltages at nodes U, W, R, S.

* If $V_R = 5V$ and $V_u = 5V$
  + 2pts each
* If $V_R = 0V$ and $V_u = 0V$
  2pts for V_u 0pt for V_R
* If $V_R = 5V$ and $V_u = 0V$
  0 pt for both

no: 5 ↑ 0 ; 0 ↑ 0 ok

2pts V_U = 5V
2pts V_W = 0V
2pts V_R = 5V
2pts V_S = 0V


5V
metal
0V
5V
R
5V
5V
U
0V
S
0V
W
5V
0V
n+
p+
p+
n+
n+
p+
n+
n+
p+
Poly
n-well
p-Si

Problem 2 (20 points)

Shown on the opposite page is the layout and two cross-sections through a CMOS inverter. A list of components follows. You are to indicate, by labelling, the location of that feature on the figure. The first question is used as an example.

2.1 Layout

(1) A contact to polysilicon [EXAMPLE]
(2) gate of NMOS transistor
(3) the W dimension of the PMOS transistor
(4) contact to p-type substrate
(5) metal contact to PMOS gate
(6) spacing from n+ source gain areas to well mask
(7) input electrode
(8) output electrode

2.2 Cross-sections

(a) well region
(b) field oxide
(c) NMOS gate oxide
(d) metal contact to PMOS source or drain
(e) poly on field oxide
(f) metal over field oxide
(g) contact to NMOS source or drain
(h) oxide over polysilicon gate

2.3 Masks

A possible list of masks for this process follows. You are to order the masks by simply filling in the mask number. It is possible that one or more masks is missing. If so, you must fill out a new mask row for each missing mask.

	MASK#	NAME	FUNCTION
	(3)	Poly	Define polysilicon areas
or (5)	(4)	N-select	Define n+ implant areas
(4)	(5)	P-select	Define p+ implant areas
	(2)	Oxide	Define areas for gate oxide
	(7)	Metal	Define metal conductor pattern
	(1)	WELL	DEFINE N-WELL
Fill in mask # here →	(6)	CONTACT	DEFINE CONTACT OPENINGS

2.4 Gate delay

For this layout, what do we expect for the relationship between gate delay for output rising (t_{pLH}), and output falling (t_{pHL})? Answer by putting in the correct symbol in the box (=, >, or <).

Put symbol here →

t_{pLH} [>] t_{pHL}

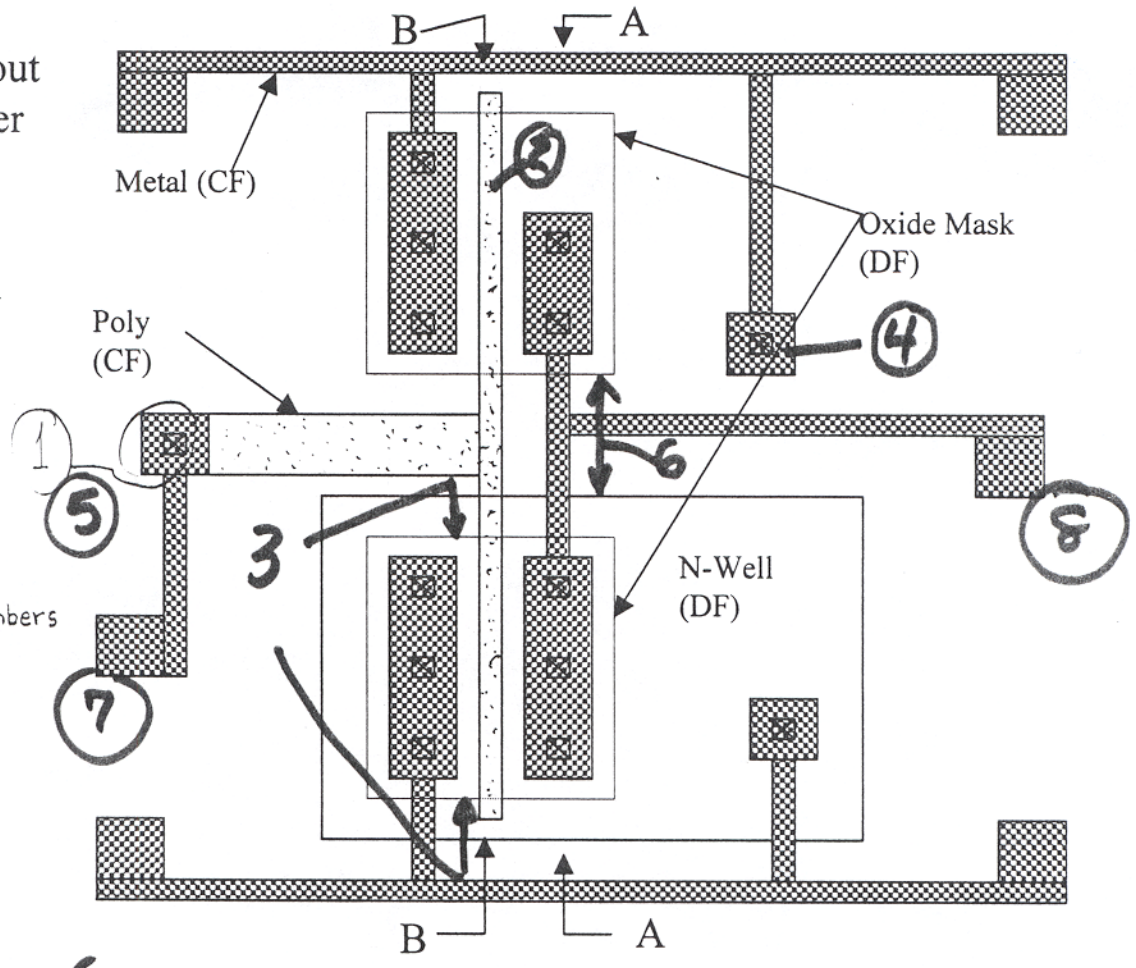
Why? PMOS $R_p > R_N \Rightarrow t_{pLH}$ LONGER

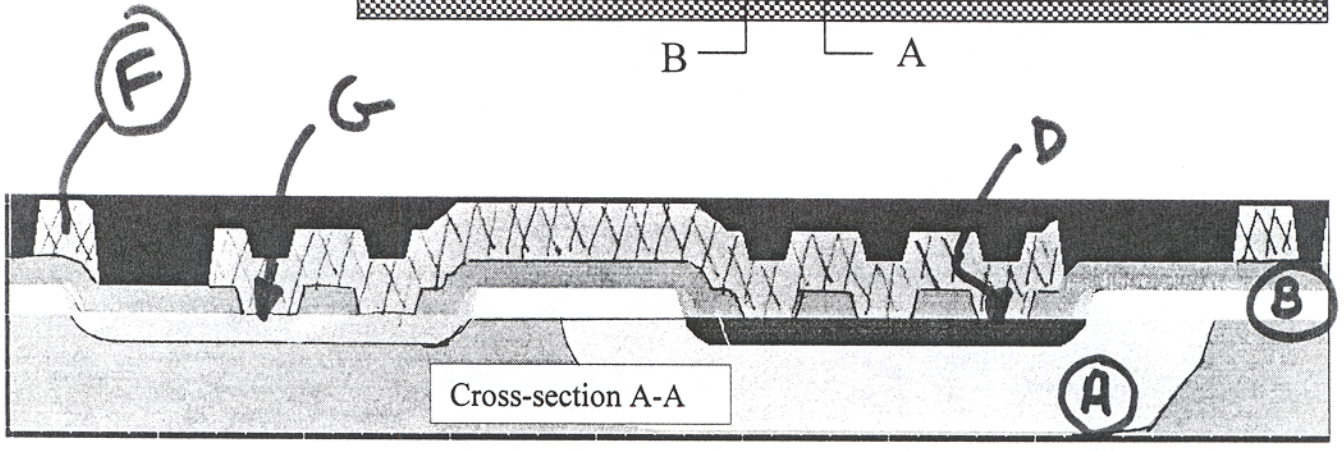
CMOS INVERTER

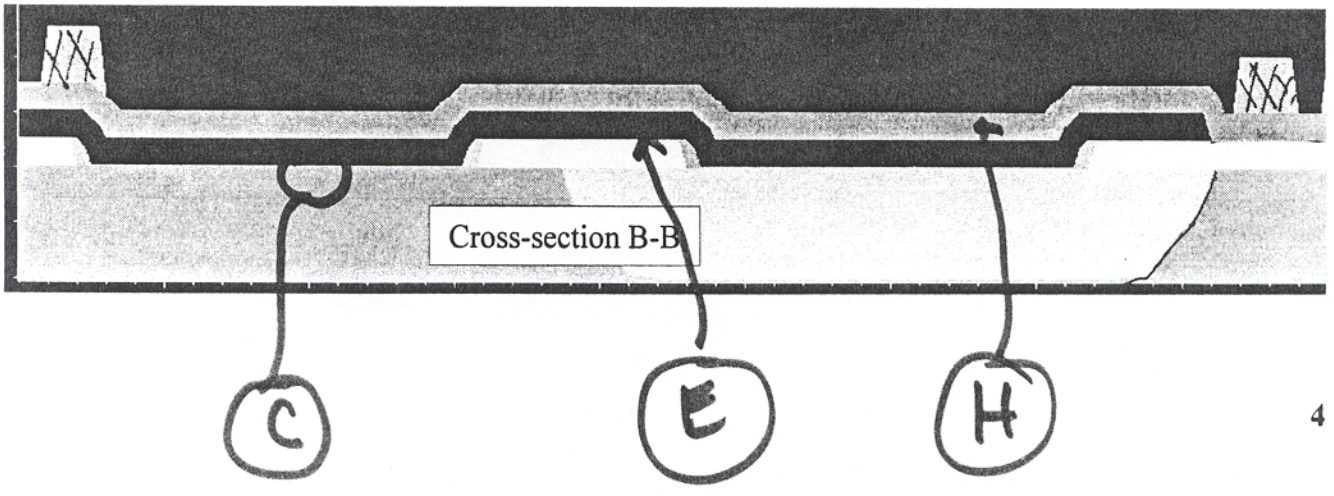
Redrawn Layout from SIMPLer

CF=Clear Field,
DF = Dark Field

NOTE! In answering this question, put numbers ONLY on layout, and only letters on cross-sections

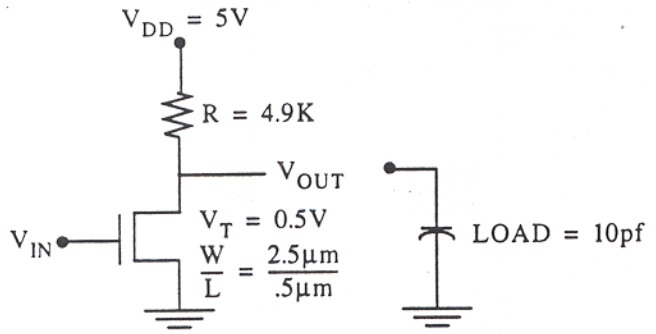






Problem 3 (20 points)

You are trying to construct a dc switch with an MOS transistor, as shown below. The idea: When input is low, output high. But when input is high, output is hopefully low.



Note: For this transistor

$C_{ox} = 10fF/\mu m^2 = 1\mu F/cm^2$

$\mu = 1000 \frac{cm^2}{V\ sec}$ for electrons

(a) If $V_{IN} = 5V$, what is the channel electron charge (coulomb/cm^2)(for small values of V_{OUT} only)?

$Q = C_{ox}(V_{GS} - V_T)$

10^{-6} 5 .5

formula $C_{ox}(V_{GS} - V_T)$

value 4.5×10^{-6}

(b) If $V_{IN} = 5\ V$, what is the sheet resistance of the channel? (Again for the case in which V_{OUT} is very small.)

$R_\square = \frac{1}{\mu Q}$

1000 4.5×10^{-6}

formula $1/\mu Q$

value 222 Ω/□

(c) What is the value of V_{IN} needed to produce an output of 0.1 V?

5V, 4.9K, .1V, X $\Rightarrow \frac{X}{4.9+X} \times 5 = .1 \Rightarrow X = .1K$

$V_{IN} =$ 2.5 V

$R = R_\square \times \frac{L}{W} \leftarrow \frac{1}{5} \Rightarrow R_\square = 500\ \Omega/\square$

100

$\Rightarrow V_{GS} - V_T = 2V$

(d) If the input suddenly switches low, and the load is 10 pF, as shown, sketch the output voltage versus time (accurately) and estimate the time Δt for the output to go from 0.1 V to 2.45V (halfway to 5 V).

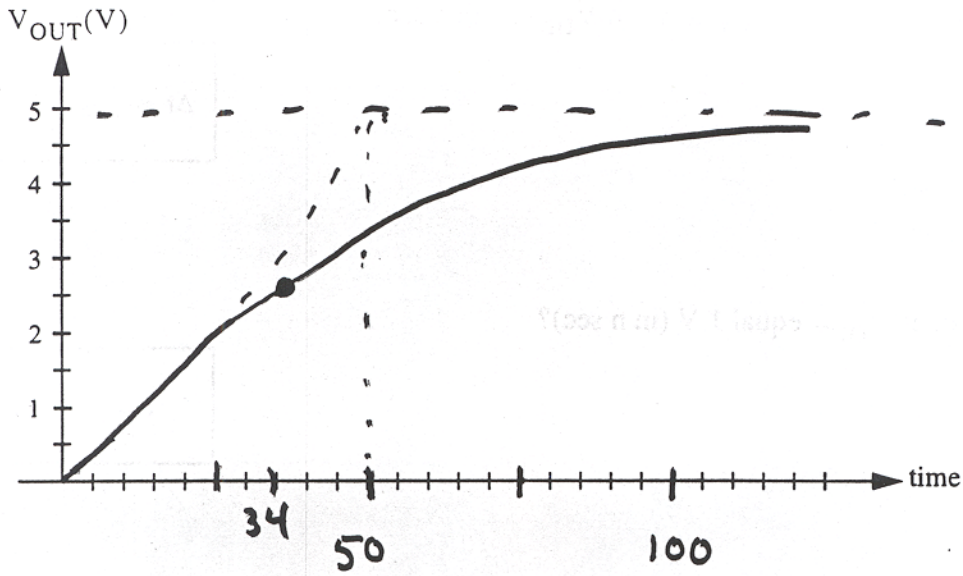
HALF-WAY $\Rightarrow \Delta t = .69\ RC$

4.9K 10pF

$\Delta t =$ 33.8 n sec

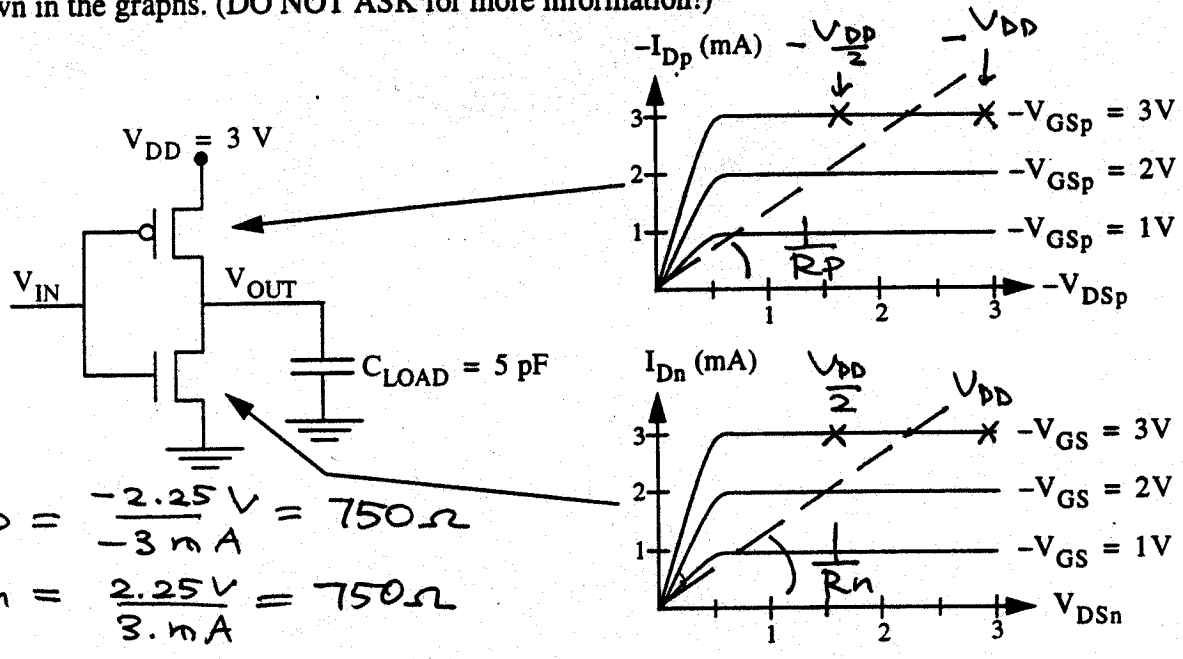
Problem 3 Answer Sheet

(d)



Problem 4 (20 points)

A CMOS inverter drives an off-chip capacitance load, as shown below. All you know about the MOS transistors is shown in the graphs. (DO NOT ASK for more information!)



$$Rp = \frac{-2.25\,V}{-3\,mA} = 750\Omega$$

$$Rn = \frac{2.25\,V}{3.\,mA} = 750\Omega$$

(a) Draw the circuit model (in the box provided on opposite page) for the circuit (replacing transistors with appropriate simpler elements, such as voltage sources, current sources, resistors, capacitors, inductors) when V_{IN} = 3V. No numerical values are required in part (a).

(b) Suppose V_{IN} suddenly switches to 0V at $t = 0^+$. Draw the new circuit model in the box provided (again with simpler elements). Show both the general form and the numerical values for all parameters.

(c) Sketch the form of V_{OUT} versus time for $t = 0^+$ to $t \to \infty$ on the axes provided. (No numbers needed.)

(d) What is the time delay for V_{OUT} to go to $V_{DD}/2$ (in n sec)?

$$\tau = R_p \times C_{LOAD}$$

$$0.69\,\tau = 2.59\,ns$$

Δt = 2.59 nsec

(e) At what time does V_{OUT} equal 1 V (in n sec)?

$$V_{out}(t) = 3 - 3e^{-t/\tau}$$

$$1\,V = 3 - 3e^{-t/\tau}\,V$$

$$t = 0.4 \times \tau$$

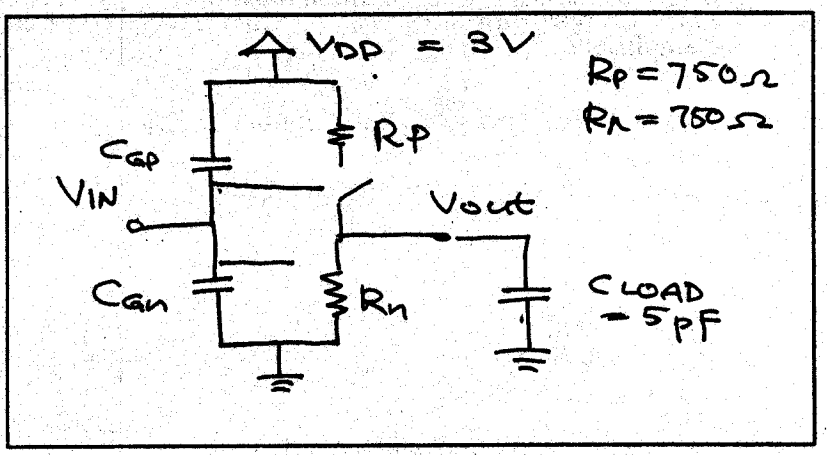
$$= 1.52\,ns$$

t = 1.52 nsec

Prob. 4 Answer Sheet (Parts a, b, c)

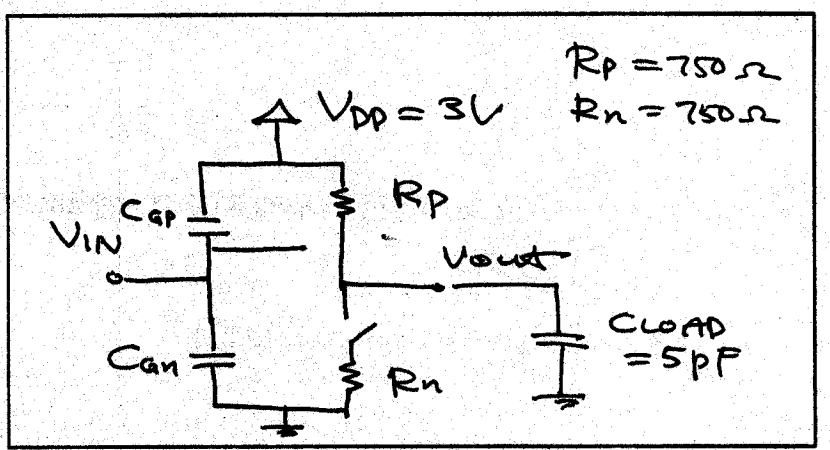
(a)

PUT CIRCUIT HERE → for $V_{IN} = 3V$

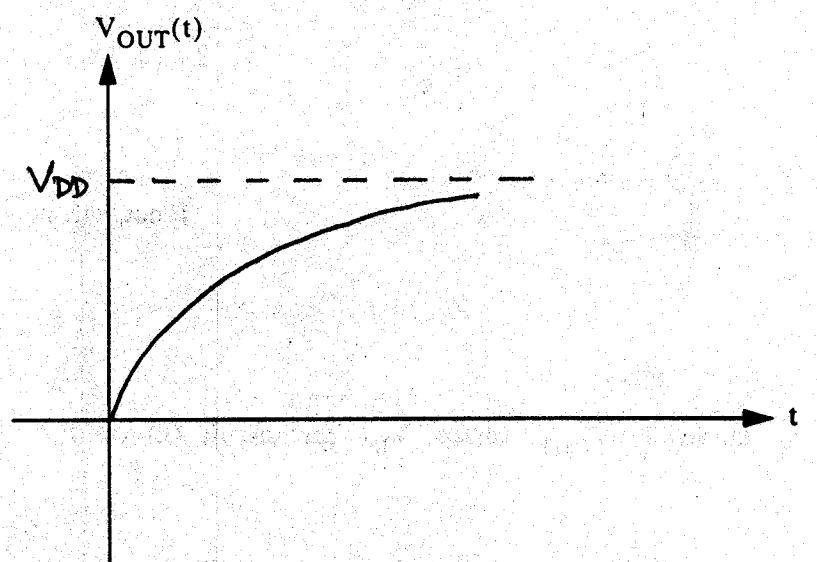


(b)

PUT CIRCUIT HERE → for $V_{IN} = 0$



(c)



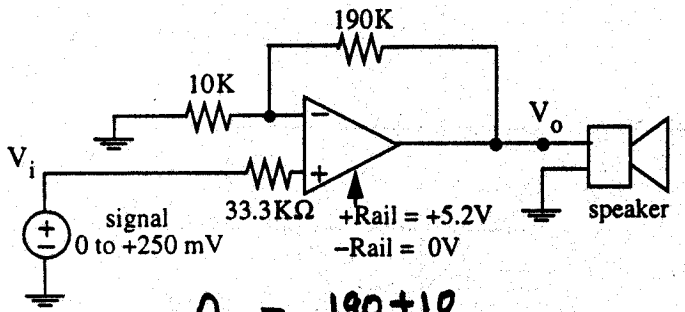
Problem 5 (20 points)

(a) You open up your Robot Kit and find the following circuit. You suspect it is a linear voltage amplifier. You know the differential amplifier has very high internal gain.

(a.1) Is it a linear amplifier?

(a.2) If so, what is the voltage gain $\frac{V_o}{V_i}$? [If not, ignore (a.2).]

(a.3) If not, why not?



$A_V = \frac{190+10}{10} = 20$

Linear amplifier? (Yes or No)

$A_V \equiv \frac{V_o}{V_i} = 20$

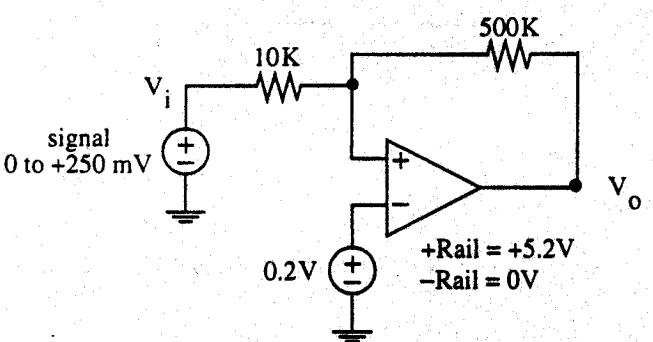
If not, why not?_____

(b) You also find the following circuit. Again you suspect a linear amplifier. You know the differential amplifier has very high internal gain.

(b.1) Is it a linear amplifier?

(b.2) If so, what is the voltage gain? [If not, ignore (b.2).]

(b.3) If not, why not?



Linear amplifier? (Yes or No)

$A_V \equiv \frac{V_o}{V_i} =$ _____

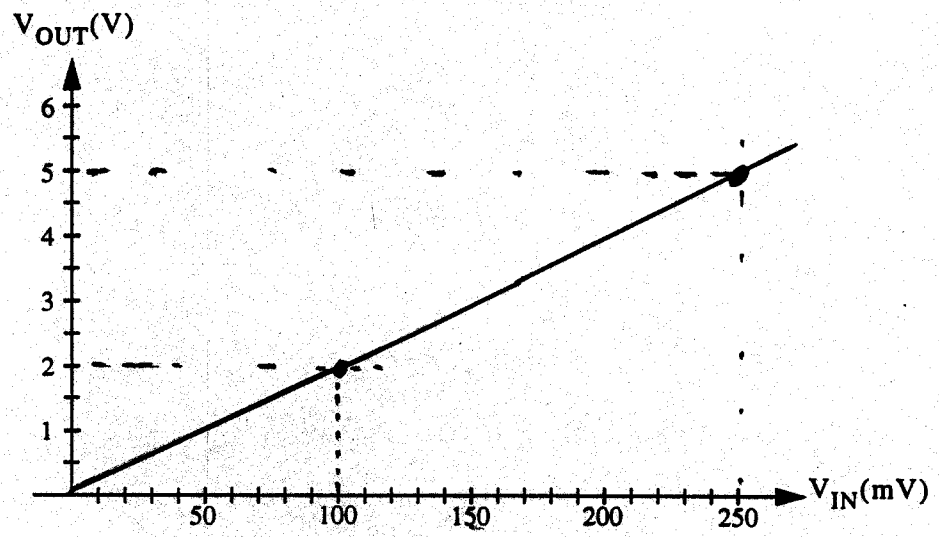
If not, why not? + FEEDBACK (AT RAILS)

(c) Carefully sketch the curve of V_{OUT} versus V_{IN} for circuit (a) on the graph axes provided for $0 \le V_i \le 250\text{mV}$.

(d) Carefully sketch the curve of V_{OUT} versus V_{IN} for circuit (b) on the graph axes provided for $0 \le V_i \le 250\text{mV}$.

Prob. 5. Answer Sheet

(c)



(d)

IF V_o HIGH

V_i — 10K — X — 500K — 5.2

$V_X = V_i + \frac{10}{510}\cdot(5.2 - V_i) \Rightarrow V_i = 0.1V$

IF V_o LOW:

$V_X = \frac{500}{510} V_i$

V_i — 10K — X — 500K — ⏚

V_X = SWITCH AT OF 0.2V WHEN V_i = .204 V