Name ____Solutions_____

EE40

Midterm 3

April 24, 2003

PLEASE WRITE YOUR NAME ON EACH ATTACHED PAGE

PLEASE SHOW YOUR WORK TO RECEIVE PARTIAL CREDIT

PLEASE DO NOT LEAVE UNTIL EXAM PERIOD IS OVER

Problem 1: 15 Points Possible _____

Problem 2: 20 Points Possible _____

Problem 3: 15 Points Possible _____

Problem 4: 20 Points Possible _____

Problem 5: 20 Points Possible _____

Problem 6: 10 Points Possible _____

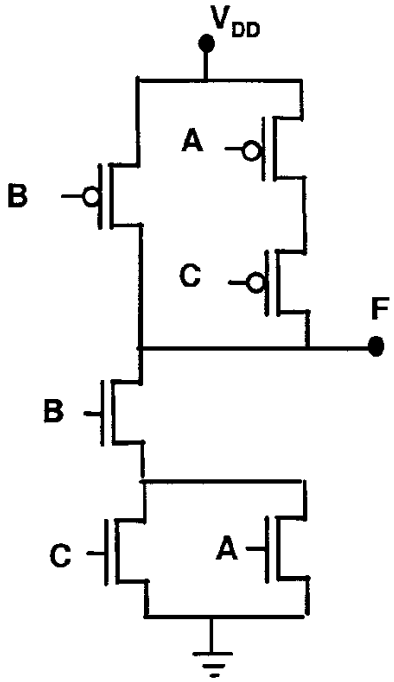
TOTAL: 100 Points Possible _____

Name ____Solutions_____

Problem 1: 15 Points Possible

Determine whether the circuit below performs a logical operation. If it does, give the Boolean function it computes. If not, give a set of inputs that results in an invalid output.

For your convenience, 8 copies of this circuit are given on the next page. Assume that all PMOS transistors have source terminal on top, and all NMOS transistors have source terminal on the bottom.



From looking at PMOS half: $F = V_{DD}$ if B conducts OR (A conducts AND C conducts)

$F = \overline{B} + \overline{A}\,\overline{C}$

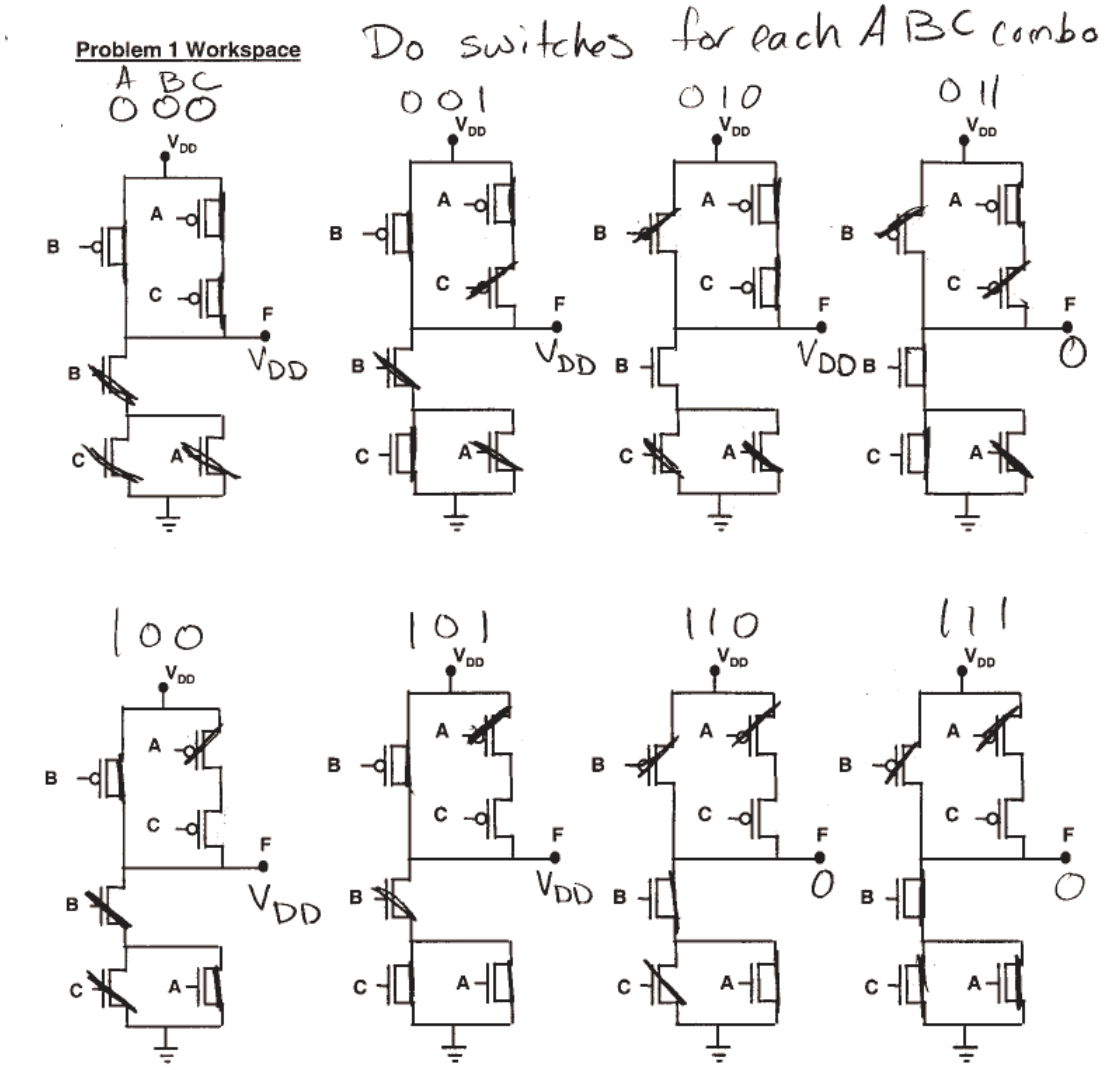
From looking at NMOS half: $F = 0$ if B conducts AND (A conducts OR C conducts)

$\overline{F} = B(A + C)$

These agree by DeMorgan's law; it is a logic circuit.

Name ____Solutions_____

Problem 1 Workspace



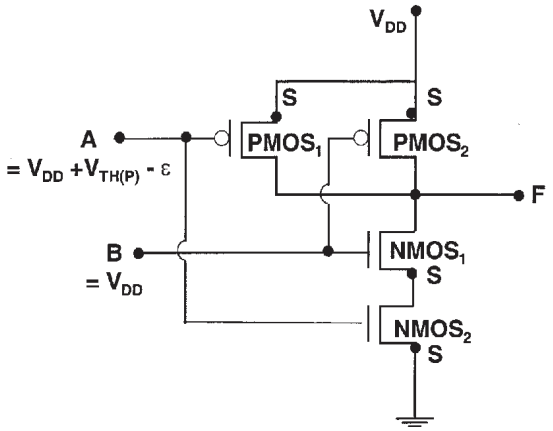
$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$

(Equivalent to previous results).

Name ____Solutions_____

Problem 2: 20 Points Possible

For the CMOS logic circuit below, determine the most probable mode of operation for each transistor. Assume that ε is a very small positive number, and V_{DD} is much larger in magnitude than either V_{TH} .



$PMOS_2$ cutoff ($V_{GSP2} = V_{DD} - V_{DD} = 0V$)

$PMOS_1$ barely on ($V_{GSP1} = V_{DD} + V_{THP} - \varepsilon - V_{DD} = V_{THP} - \varepsilon$)

I_D shared by $PMOS_1$, $NMOS_1$, $NMOS_2$ is small

$V_{GSN2} = V_{DD} + V_{THP} - \varepsilon$ for $NMOS_2$ is not small and is positive, since V_{DD} is much larger in magnitude than V_{THP} or ε (by assumption).

$NMOS_2$ fully on with small $I_D \Rightarrow$ $NMOS_2$ triode

$NMOS_2$ therefore also has small V_{DSN2},

so $V_{GSN1} = V_{DD} - V_{DSN2}$, the gate-source voltage for $NMOS_1$ is not small. $NMOS_1$ fully on, small $I_D \Rightarrow$ $NMOS_1$ triode

$NMOS_1$ therefore has small V_{DSN1}.

$$V_{DD} = \underbrace{V_{DSN1}}_{\text{small}} + \underbrace{V_{DSN2}}_{\text{small}} - V_{DSP1}$$

$\Rightarrow$ V_{DSP1} negative with large magnitude

V_{GSP1} negative with small magnitude & V_{DSP1} negative with large magnitude $\Rightarrow$ $PMOS_1$ saturation

Name ____Solutions_____

Problem 3: 15 Points Possible

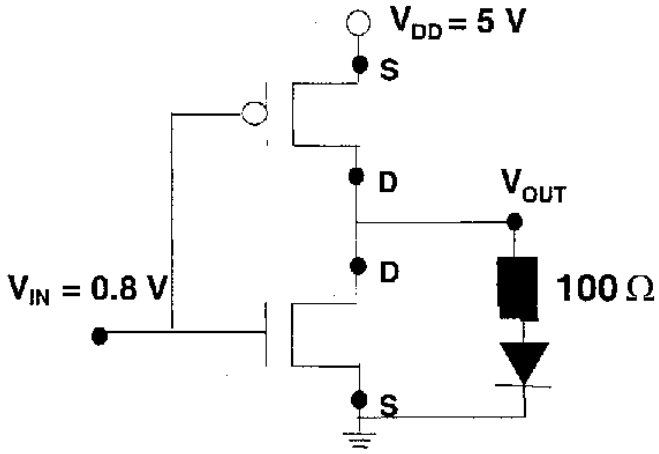
Consider the inverter at right, which turns on an LED when the output voltage is high.

I have put a resistor in series with the LED to limit the current so the LED doesn't burn.

But, the LED needs a current of at least 20 mA to light up.

I want the LED to light up for an input voltage as high as 0.8 V.

Will the LED light up for an input of 0.8 V?



$W/L\ \mu C_{OX}$ = 100 mA/V^2 for both transistors,
$V_{TH(N)} = -V_{TH(P)}$ = 1 V,
λ = 0 V^{-1} for both transistors,
V_F = 2 V for the LED (use large-signal model).

NMOS cutoff ($V_{GSN} = V_{IN} = 0.8\ V$) $\Rightarrow I_{DN} = 0A$

PMOS triode (will show PMOS sat. is wrong)

① $I_{Dp} = -100 mA/V^2 (\underbrace{0.8V - 5V - -1V}_{V_{GSP}} - \frac{V_{DSP}}{2}) V_{DSP}$

By KVL, ② $V_{DSP} = V_{OUT} - V_{DD} = V_{OUT} - 5$

By KCL, ③ $I_{Dp} = -\frac{V_{OUT} - V_F}{100} = -\frac{V_{OUT} - 2V}{100}$

Put ③ and ② into ① and solve for V_{out}:

$V_{out} = \{-1.51\ V, 4.91\ V\}$
impossible! keep.

$V_{DSP} = -0.09V$ OK for triode mode.

$I_{diode} = \frac{V_{out} - 2V}{100\Omega} = 29.1\ mA$ (LED Lights up!)

If guessed saturation for PMOS,

$I_{Dp} = -\frac{1}{2} \cdot 100\ mA\ (0.8V - 5V - -1V)^2$
$= -512\ mA$

$V_{DSP} = V_{out} - V_{DD} = -100 I_{Dp} + 2V - 5V$
$= 48.2\ V$ whoa! impossible.

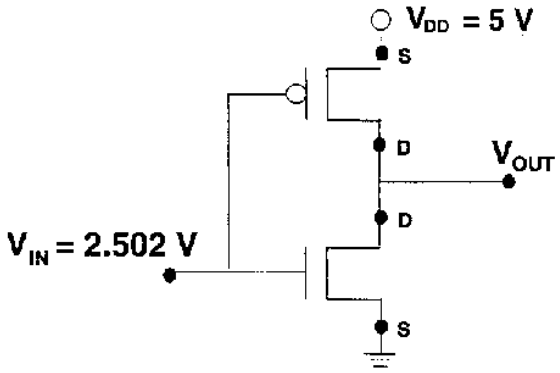
Name ____Solutions_____

Problem 4: 20 Points Possible

Consider the CMOS inverter at right, with

W/L μ C_{OX} = 1 mA/V^2 for both transistors,
$V_{TH(N)} = -V_{TH(P)}$ = 1 V,
λ = **0.01 V^{-1} for both transistors.**

For this inverter, V_M = 2.5 V.



a) Find V_{OUT} for V_{IN} = 2.502 V. Hint for guessing modes: Notice that V_{IN} is close to V_M.

b) Find the slope of the V_{OUT} vs. V_{IN} curve in this region, given by

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{V_{OUT}(\text{for } V_{IN} = 2.502\text{ V}) - V_M}{2.502\text{ V} - V_M}$$

Since we have unloaded inverter with V_{in} close to V_M, assume "region C" with both transistors in saturation.

$I_{DN} = \frac{1}{2} \cdot 1\text{mA/V}^2 (2.502\text{V} - 1\text{V})^2 (1 + 0.01 V_{DSN})$

$I_{DP} = -\frac{1}{2} \cdot 1\text{mA/V}^2 (2.502\text{V} - 5\text{V} - -1\text{V})^2 (1 - 0.01 V_{DSP})$

KVL: $V_{DSP} = V_{DSN} - V_{DD} = V_{DSN} - 5\text{V}$

KCL: $I_{DP} + I_{DN} = 0 \Rightarrow I_{DN} = -I_{DP}$

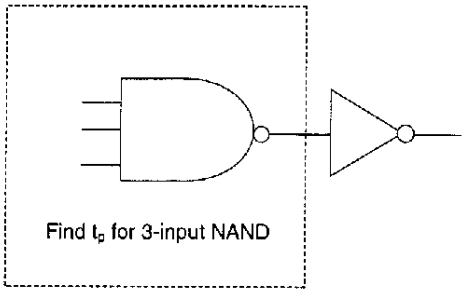
Solve the above to get $V_{DSN} = V_{OUT} = 2.23\text{ V}$

$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{2.23\text{V} - 2.5\text{V}}{2.502\text{V} - 2.5\text{V}} = -135$

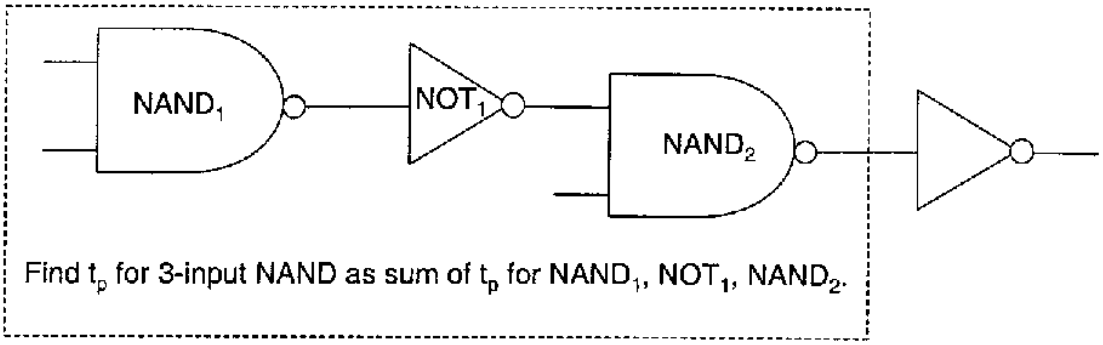
Name ____Solutions_____

Problem 5: 20 Points Possible

Find the propagation delay for this 3-input NAND gate with inverter load,



where the 3-input NAND is implemented using two 2-input NAND gates and an inverter:



Compute the propagation delay t_p for the 3-input NAND as the sum of the worst-case propagation delays of the individual gates inside.

Use R_N = 1 kΩ, R_P = 2 kΩ, and C_G = 10 fF per transistor. Ignore interconnect capacitance.

$NAND_1$: $t_p = 0.69 R_p (2C_G)$ = 27.6 ps

Same for $NAND_2$.

Worst-case resistance is $2R_N$ or R_p (equal)

$C_{out} = 2C_G$ (inverter has 2 transistors)

NOT_1: $t_p = 0.69 R_p (2C_G)$ = 27.6 ps

Total t_p for 3-input NAND: 3(27.6 ps) = 82.8 ps

Worst-case resistance is R_p.

$C_{out} = 2C_G$ (output goes to one input of NAND: 2 of the 4 transistors)

Name ____Solutions_____

Problem 6: 10 Points Possible

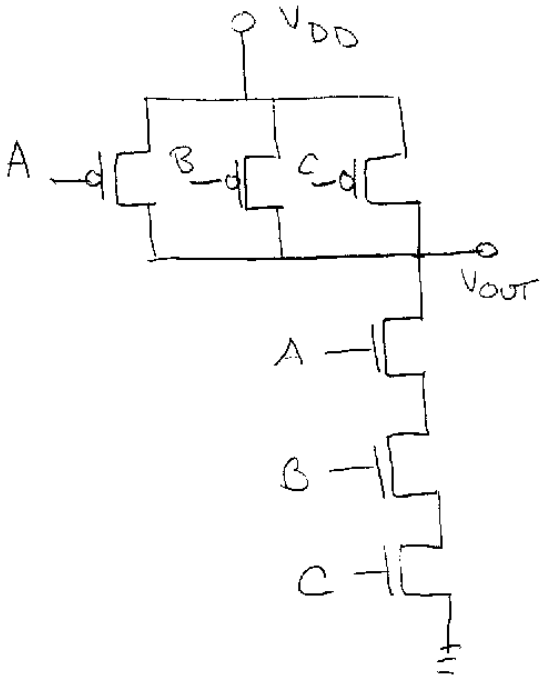
Design a circuit, using only NMOS and PMOS transistors (and a power supply), that performs the 3-input NAND function with **shorter** worse-case propagation delay than the implementation given in Problem 5, when a single inverter is attached as the output load.

Assume that your transistors have the same characteristics as those I Problem 5.

Use R_N = 1 kΩ, R_P = 2 kΩ, and C_G = 10 fF per transistor. Ignore interconnect capacitance.

Provide your design and its worst-case propagation delay with single inverter output load.

Popular Solution:



Worst-case resistance:
$3R_N$ (pull-down)
If attached to inverter,
$C_{OUT} = 2C_G$
$t_p = 0.69(3R_N)(2C_G)$
$= 41.4$ ps
(half the delay of the Problem 5 analysis)

Name ____Solutions_____

Fun Corner

It's picture time again! If you finish early, please don't get up and disturb students in your row. Instead, show off your artistic/comedic ability here.